Layer-by-layer assembled charge-trap memory devices with adjustable electronic properties

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We describe a versatile approach for preparing flash memory devices composed of polyelectrolyte/gold nanoparticle multilayer films. Anionic gold nanoparticles were used as the charge storage elements, and poly(allylamine)/poly(styrenesulfonate) multilayers deposited onto hafnium oxide (HfO_2)-coated silicon substrates formed the insulating layers. The top contact was formed by depositing HfO_2 and platinum. In this study, we investigated the effect of increasing the number of polyelectrolyte and gold nanoparticle layers on memory performance, including the size of the memory window (the critical voltage difference between the 'programmed' and 'erased' states of the devices) and programming speed. We observed a maximum memory window of about 1.8 V, with a stored electron density of 4.2×10^{12} cm^{-2} in the gold nanoparticle layers, when the devices consist of three polyelectrolyte/gold nanoparticle layers. The reported approach offers new opportunities to prepare nanostructured polyelectrolyte/gold nanoparticle-based memory devices with tailored performance.

Non-volatile flash memory devices with discrete charge-trapping layers are currently attracting significant attention due to the widespread use of portable electronic devices[1–3]. Recently, the fabrication of a 32-gigabit silicon-oxide-nitride-oxide-silicon (SONOS) type flash memory device using Si_3N_4 as a charge-trap layer was reported[4]. However, in these devices, it can be difficult to control the charge trap density and distribution. In contrast, flash memory devices that use metallic or semiconductor nanoparticles as charge-trapping elements allow the number density and distribution of nanoparticles to be improved through the nanoparticle formation processes, such as ultrathin metallic film deposition or ion implantation[5,6].

In particular, the layer-by-layer (LbL) assembly method offers diverse opportunities to prepare organic/metallic composite films with tailored electrical properties and could be useful for fabricating nanoparticle-based memory devices. An important advantage of the LbL method is that it enables the preparation of films from various organic and/or inorganic components with controlled thickness and on substrates of different size, shape and functionality[7–13]. This is achieved by tuning the complementary (electrostatic, hydrogen bonding or covalent bonding) interactions between the various components. In addition, the technique permits the memory capacity of flash memory devices to be increased through deposition of multiple layers, differing from other devices that only use a single layer[3,5,6,14–19].

We use the LbL approach to assemble polyelectrolyte/gold nanoparticle (PE/Au_{NP}) multilayer films on silicon (Si) substrates precoated with a tunnelling oxide layer to prepare flash memory devices with (1) tailored nanostructures, (2) a defined number density of charge-trap elements, and (3) tailored electrical properties. The importance of this work resides in the fact that we can significantly increase the memory capacity per unit area by increasing the number of PE/Au_{NP} layers and still use the same device architecture and semiconductor processing that is the basis of existing charge-trap flash memory devices.

RESULTS AND DISCUSSION

Quartz crystal microgravimetry (QCM) measurements were conducted to quantify the adsorbed amount of citrate-stabilized Au_{NP} in the (PE/Au_{NP})$_n$ multilayer films. Figure 1a shows the frequency change, $-\Delta F$, and the mass change of adsorbed Au_{NP} and PEs with increasing periodic layer number n. These QCM frequency (or mass) changes indicate that regular multilayer film growth occurs when metallic Au_{NP} and organic PEs are LbL-assembled from the deposition solutions. The change in number density of adsorbed Au_{NP} as a function of n can be obtained by calculating the mass of an Au_{NP} sphere with a diameter of 16 nm and density of 19.3 g cm^{-3}, as shown in the inset of Fig. 1a.

We used 16-nm Au_{NP} to ensure that the nanoparticles were metallic without gold oxide[20] and to avoid the quantum size effects that become pronounced in Au_{NP} below 4 nm (see Supplementary Information, Fig. S1; ref. 21). However, we note that Au_{NP} with unique shapes[22], such as nanorods, should be similarly applicable to our system provided they have similar surface characteristics and do not exhibit quantum size effects.

Scanning electron microscopy (SEM) images of the structure of the (PE/Au_{NP})$_n$ multilayers for $n = 1–4$ are shown in Fig. 1b–e.

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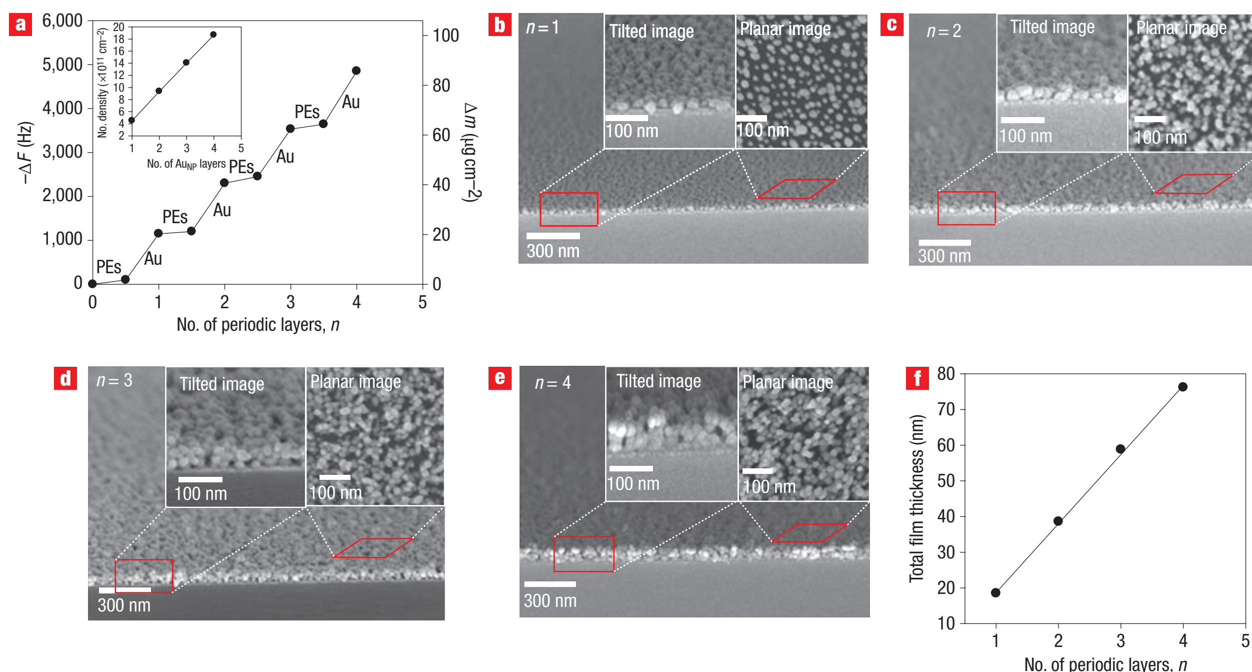

Figure 1 Thickness and charge density measurements of $(PE/Au_{NP})_n$ multilayers for $n = 1$–4. a, Frequency change of a quartz crystal oscillator (left axis) and corresponding change in adsorbed mass of PEs and Au_{NP} (right axis) as a function of periodic layer number n. The inset shows the change in number density of Au_{NP} within the multilayers. **b**–**e**, SEM images of the cross-section of $(PE/Au_{NP})_n$ multilayer films for $n = 1$ (**b**), $n = 2$ (**c**), $n = 3$ (**d**) and $n = 4$ (**e**). The insets of **b**–**e** show the tilted (left side) and planar (right side) images magnified from areas indicated by the two different red boxes. **f**, The total film thicknesses of the $(PE/Au_{NP})_n$ multilayers are 19.0 nm, 39.5 nm, 60.2 nm and 78.3 nm for $n = 1$, 2, 3 and 4, respectively.

The adsorbed Au_{NP} in the multilayer films are well dispersed and discontinuous due to the electrostatic repulsion between neighbouring Au_{NP} in the same layer and the 4-nm-thick PE layers inserted between each of the different Au_{NP} layers. The total film thickness of the multilayers increased from 19.0 to 78.3 nm when increasing n from 1 to 4 (Fig. 1f). These observations indicate that the Au_{NP} within the multilayer films can be operated as isolated charge-storage elements. Additionally, these LbL-multilayer films based on a dipping process can be easily and rapidly prepared by the LbL-assembly process based on spin-coating (see Supplementary Information, Fig. S2; refs 23–26).

The LbL technique was used to fabricate flash memory devices composed of $(PE/Au_{NP})_n$ multilayer films sandwiched between a tunnelling oxide (HfO_2) (grown on silicon) and a blocking oxide (HfO_2) connected to a Pt electrode (Fig. 2). To measure the amount of stored charge on the devices, we measured the capacitance responses of the multilayers as a function of a voltage applied between the Pt electrode and the silicon substrate. The measurements were performed at 1 MHz to avoid the frequency dependence in dielectric properties found by us and others[27] in these PE materials below 1 kHz (see Supplementary Information, Fig. S3). For the PE films, some frequency dependency was observed below hundreds of Hz, but this was not seen above 1 kHz.

Capacitance/voltage (C–V) curves for the 'as-grown' $(PE/Au_{NP})_{n\approx1-4}$ multilayered devices were obtained by scanning the applied voltage from −4 to 2 V, and back to −4 V, as shown in Fig. 3a. This characterizes the initial state of the devices. Within this voltage range, we found that these devices had no charging effects as they showed negligible hysteresis in the C–V curves. Capacitance values in the accumulation region (at a negative bias) decreased from 23 to 16.3 pF, and the entire curve

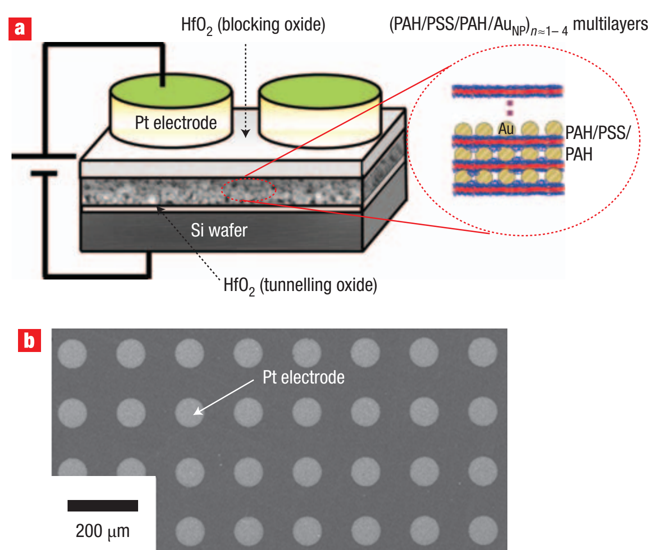

Figure 2 Structure of a typical memory device prepared with the LbL technique. a, Perspective view of two devices (defined by the Pt electrodes). **b**, Top-view SEM image of a device array.

shifted to positive voltage with increasing PE thickness. The shift implies that the Au_{NP} number density increases with increasing n and that the Au_{NP} are electrically charged in their initial states.

In the following, a 'programmed' device is one in which there is finite charge stored within the charge-trap elements (that is, Au_{NP}),

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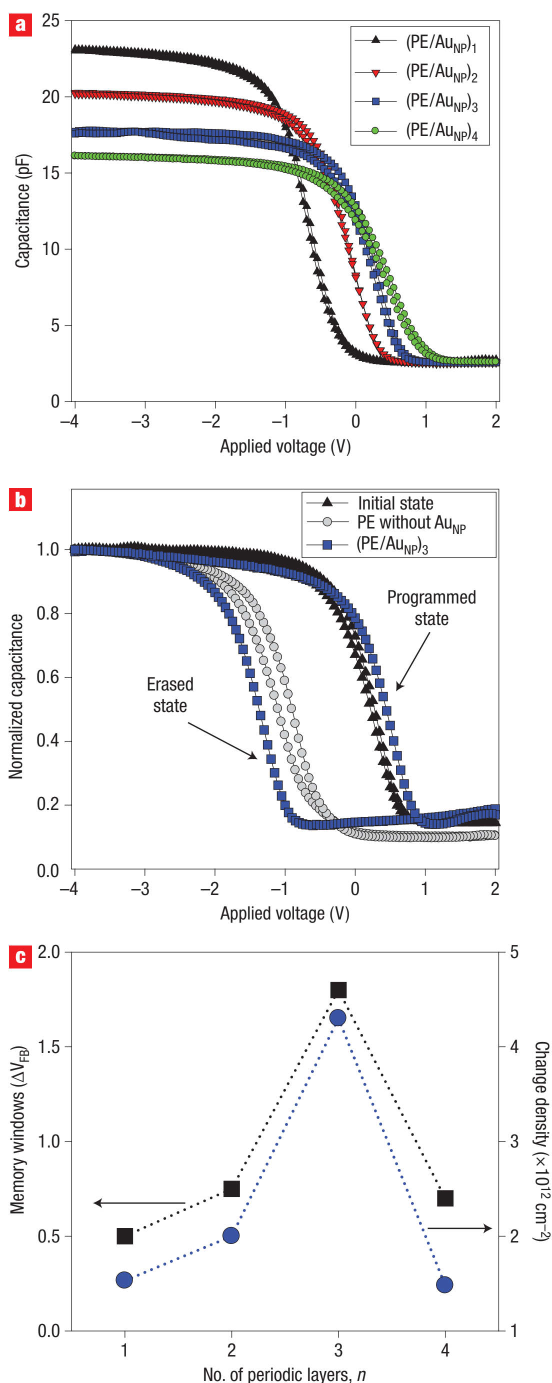

Figure 3 Capacitance versus voltage (C–V) curves for $(PE/Au_{NP})_n$ multilayers for $n = 1$–4. a, C–V curves for multilayers in the initial state were measured by scanning the voltage from −4 V to 2 V and back to −4 V. **b**, C–V hysteresis curves for a $(PE/Au_{NP})_3$ device in the initial state (the black triangles) and after applying the programming/erasing voltages (the left and right sides of the C–V curves of filled squares represent the erased and programmed states of the memory devices obtained after applying −8 V and 20 V to the Pt gate electrode, respectively). The curve of grey circles corresponds to a $(PE)_4$ device without Au_{NP}. **c**, Plot of the change in memory window and the stored charge-carrier density with increasing n. The charge density Q stored within the Au_{NP} can be estimated using the equation $Q = C\Delta V_{FB}$, where C is the capacitance per unit area and memory windows are defined as $\Delta V_{FB} = V_{FB}$ (program)$-V_{FB}$ (erase).

whereas an 'erased' device is referred to a memory state after the charges stored within the Au_{NP} are moved to the Si substrate. From the measurements of the C–V responses according to the programming/erasing operations, we can measure the critical voltage change between the programmed and erased states of the memory devices, which is defined as the memory window. Devices are 'programmed' by applying a bias voltage of 20 V for 30 ms and 'erased' by applying an erase voltage of −8 V for 10 ms.

The tunnelling oxide thickness was varied from 0.9 to 1.9 nm, and it was found that a thickness of 1.4 nm provided a reasonable compromise between the program/erase speed (favoured by a thinner oxide) and the data retention capability (favoured by a thicker oxide) (see Supplementary Information, Fig. S4). Using this optimum oxide thickness of 1.4 nm, we investigated the role of Au_{NP} as charge-storage elements in the multilayered devices. As shown in Fig. 3b, a device without Au_{NP} displayed a negligible memory effect (memory window of less than 0.2 V) even though program and erase voltages of 20 V for 30 ms and −8 V for 10 ms, respectively, had been applied. In contrast, the multilayered device embedded with Au_{NP} displayed a memory window of about 1.8 V under the same conditions. These results show that Au_{NP} have a significant role as charge-storage elements, and insulating PE layers have a negligible effect on charging properties. Additionally, the erase operating voltage (−8 V) for these devices is low compared to conventional flash memory devices (for example, the SONOS type).

Figure 3c shows how memory window and stored charge density, measured from the C–V curves, depend on the number of periodic layers n. The memory windows increased from 0.5 to 1.8 V when the number density of Au_{NP} increased from 4.5×10^{11} cm^{-2} (for $n = 1$) to 1.4×10^{12} cm^{-2} (for $n = 3$). For the $(PE/Au_{NP})_4$ device, the memory window was smaller (about 0.7 V) compared to the $(PE/Au_{NP})_3$ device, despite increasing the number density of Au_{NP}. The electric field across the $(PE/Au_{NP})_{n\approx 1-4}$ devices decreases inversely proportionally to the total film thickness of the $(PE/Au_{NP})_{n\approx 1-4}$ multilayers. Therefore, the memory windows are expected to be enhanced with increasing periodic layer number under the same electric field, as the number density of Au_{NP} as charge-storage elements also increases. The charge carrier density Q stored within the Au_{NP} is closely related to the magnitude of the memory windows, ΔV_{FB}, where subscript FB indicates flatband (Fig. 3c; ref. 17). We estimate that three or four electrons were stored in a single Au_{NP}.

For practical memory applications, a wide memory window is essential to separate the programmed and erased states. In this study, memory windows of 1.8 V have been achieved for the $(PE/Au_{NP})_3$ device with a 1.4-nm tunnelling oxide layer thickness. Although we cannot exclude the possibility that other parameters, such as the gate electrode material, dielectric layer thickness, substrate conductivities or interference between neighbouring cells, also have a significant effect on device performance, we have focused on a facile method for significantly improving charge-trapping efficiency by vertical integration of charge-trapping elements through LbL assembly.

To demonstrate the feasibility of our proposed devices in nanoscale applications, the non-volatile memory effect using modified scanning nonlinear dielectric microscopy (SNDM) was investigated[28,29]. The charges stored within the Au_{NP} can be detected from the change in the capacitance when the tip of the SNDM scans the surface of the blocking oxide layers (HfO_2) covering the Au_{NP} (see Methods section for details). It should be noted that the tip was grounded and the bias was applied to the Si substrate, so the bias polarity was reversed for programming/erasing operations in the SNDM measurement. In Fig. 4, the yellow region corresponds to the programmed state and the dark region corresponds to the erased state. In this case, the evident contrast changes of SNDM images, obtained from these

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erasing/programming operations, strongly support the fact that our device can yield flash memory characteristics on the nanometre scale (Fig. 4). Similar effects were obtained with Pt_{NP} as a charge-trap element (see Supplementary Information, Fig. S5).

For high-density devices, a narrow distribution of erased and programmed cells is important[30]. The cell distribution in nanoparticle memory devices depends mostly on the density distribution of nanoparticles[3]. In this work, the variation of Au_{NP} number density in the defined area of 0.25 μm^2 is less than 2%, as determined from analysis of SEM images for the $(PE/Au_{NP})_1$ film (see Supplementary Information, Fig. S6). This result indicates that the erased and programmed cell distribution will be less than 2%, leaving sufficient memory window separation if a variation in tunnelling and blocking oxide thickness is almost negligible. However, in order to be compatible with the homogeneity of charge-storage elements required at about the 50 nm length scale of future Si-based memory devices, the nanoparticle size should be significantly decreased. We therefore investigated the surface homogeneity of a $(PE/Pt_{NP})_1$ film at the 50 nm scale and found the cell distribution to be less than 5% (see Supplementary Information, Fig. S7).

One of the most important factors for the application of non-volatile memory devices is their charge-retention capability[30]. It was observed that there was almost no charge loss for programmed and erased cells under mild durability conditions (less than 0.2 V at room temperature for 7 days) and during an accelerated test (less than 0.3 V at 150 °C for 2 h), as measured by the relative changes in C–V curves of programmed and erased cells from their initial C–V curves before and after retention. In a previous report[14,15], we speculated that the major concern for the application of polystyrene (PS) matrices blended with Au_{NP} for non-volatile memory devices is the aggregation of Au_{NP} at temperatures above the glass transition temperature (T_g) of PS. This would result from the thermodynamically unfavourable interactions between PS and dodecanthiol-stabilized Au_{NP} with the relatively low T_g of PS (ref. 31). This phenomenon can have a fatal effect on device performance, such as retention capability at high temperature. However, our devices, which are based on poly(allylamine) (PAH)/poly(styrenesulphonate) (PSS) multilayers, maintain their retention capability at 150 °C, probably due to the formation of thermally stable bonding between the PEs and Au_{NP}, as is known for PE multilayered systems[32,33].

Electrical cycling testing between the programmed and erased states was also carried out (see Supplementary Information, Fig. S8) and the memory windows were well maintained up to tens of cycles. This property is comparable with those already reported[15,16].

Considering the energy band structures of the $(PE/Au_{NP})_3$ memory devices, the electron barrier height for HfO_2 tunnelling oxides is significantly lower than that of SONOS-type devices with SiO_2 tunnelling oxides. Such a low barrier height improves the programming of the $(PE/Au_{NP})_3$ multilayered devices. However, the relatively low electron barrier for the blocking oxide (HfO_2) could also facilitate electron transfer from the Au_{NP} layers to the gate electrode. As a result, the low electron barrier of the blocking oxide causes a relatively slow program speed and high programming voltage, despite its thickness of about 15 nm. To overcome this, a blocking oxide with a higher charge blocking barrier (for example, Al_2O_3, $Hf_{1-x}Al_xO_3$)[30,34–36] may result in flash memory devices with improved efficiency. During the retention state of the $(PE/Au_{NP})_3$ device, the insulating PE layers inserted between Au_{NP} layers can operate as potential wells for charges stored within the Au_{NP}. These potential wells can effectively block charge loss during the retention mode, which has already been confirmed by the observation that there was almost no charge loss for programmed and erased cells.

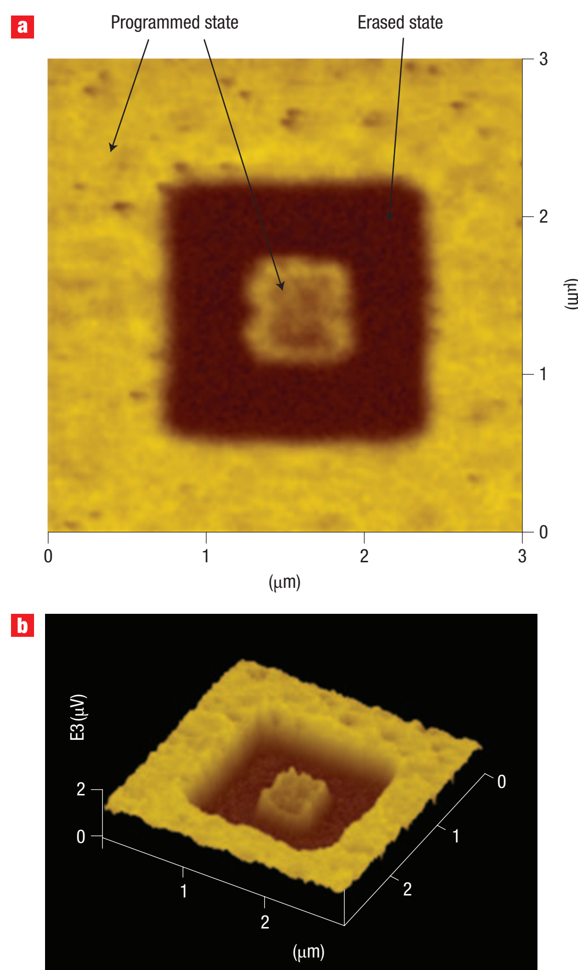

Figure 4 Real-space imaging of programmed and erased states. **a**,**b**, Two-dimensional (**a**) and three-dimensional (**b**) scanning nonlinear dielectric microscopy (SNDM) images of the $(PE/Au_{NP})_3$ multilayered devices for nanoscale measurement. It should be noted that these devices are initially programmed. First, a 3×3 μm^2 area of the device was scanned. The erase operation was performed scanning an area of 1.5×1.5 μm^2 with +6 V bias applied to the bottom contact. After this erasing process, the tip was sequentially scanned in the selected area of 500×500 nm^2 with −6 V bias applied to the bottom contact. The bias was applied to the Si substrate, but the scanning tip was grounded, so the bias polarity was reversed for programming/erasing operations in the SNDM measurement.

CONCLUSIONS

We have demonstrated that non-volatile memory devices can be prepared from LbL-assembled multilayer films composed of PEs as insulating layers and Au_{NP} as charge-trap elements. By controlling the thicknesses of the tunnelling oxide layer and the $(PE/Au_{NP})_n$ multilayers, we can significantly affect the charge transfer onto the Au_{NP}, and the memory window. We found optimum performance for the $n = 3(PE/Au_{NP})_n$ device with a 1.4-nm-thick tunnelling oxide layer, which exhibits a memory window of 1.8 V.

Our approach provides significant advantages in fabricating non-volatile flash memory devices. A variety of materials that serve as charge-trap elements can be embedded in the multilayer films using complementary interactions. Specifically, the use of 5.8-nm Pt nanoparticles (Pt_{NP}) as charge-trap elements can yield a number density above $\sim10^{13}$ cm^{-2} in four bilayers (see

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Supplementary Information, Fig. S7). In addition, the number density of the charge-trap elements can be easily controlled by the number of deposition cycles, the solution pH and/or ionic strength. For example, although the number density of adsorbed Au_{NP} in four bilayers at pH ≈ 5.6 is about 1.9×10^{12} cm^{-2}, their density can increase to above $\sim 10^{13}$ cm^{-2} by control of the solution pH and particle size (see Supplementary Information, Figs S7 and S9).

Finally, the main advantage of this technique is that memory density can be increased in the vertical and, in principle, the lateral dimensions.

METHODS

MATERIALS

Anionic PSS ($M_w = 70{,}000$) and cationic PAH ($M_w = 70{,}000$) were used as received from Aldrich. The p-type Si wafers ((100)-orientation) with a resistivity of ∼1–10 Ω-cm were purchased from Siltron. Anionic Au nanoparticles (Au_{NP}) were synthesized by the citrate reduction method[37]. Briefly, 250 ml of 2 mM $HAuCl_4$ was heated at about 70 °C with vigorous stirring. Rapid addition of 25 ml of 68 mM sodium citrate to the vortex of the solution resulted in a colour change from yellow to purple. The average diameter of the synthesized Au_{NP} was about 16 ± 2 nm. These nanoparticles, dispersed in aqueous solution of pH 5.6, have a plasmon absorption peak at 525 nm (see Supplementary Information, Fig. S10).

PREPARATION OF $(PE/AU_{NP})_n$ FILMS USING DIPPING AND SPINNING PROCESSES

The concentration of PAH and PSS solutions used for all the experiments was 1 mg ml^{-1}. HfO_2-coated Si substrates achieved an anionic surface by heating at 65 °C for 10 s in a mixture of H_2O:H_2O_2:NH_4OH = 5:1:1 vol%. These substrates were first dipped for 10 min in the cationic PAH solution (containing 0.5 M NaCl), and then washed twice by dipping in water for 1 min. Anionic PSS was subsequently deposited onto the PAH-coated substrates by using the same procedures as described above. After deposition of an additional PAH layer, anionic Au_{NP} were deposited onto the PE (PAH/PSS/PAH)-coated substrates for 60 min. This process was repeated until the desired number of layers was deposited. For the spin-assembled multilayer films, PAH solution was completely wetted on the anionic quartz substrates pretreated with RCA. The substrate was then rotated with a spinner at 4,000 r.p.m. for 20 s and the substrates thoroughly rinsed (twice) at the same speed with water[23–26]. PSS or Au_{NP} layers were also sequentially deposited onto the substrates using the same procedure as mentioned above.

QUARTZ CRYSTAL MICROGRAVIMETRY MEASUREMENTS

A QCM device (QCM200, SRS) was used to investigate the mass of material deposited after each adsorption step. The resonance frequency of the QCM electrodes was ∼5 MHz. The adsorbed mass of PEs and Au_{NP}, Δm, can be calculated from the change in QCM frequency, ΔF, according to the Sauerbrey equation[38]: ΔF (Hz) $= -56.6 \times \Delta m_A$, where Δm_A is the mass change per quartz crystal unit area, in μg cm^{-2}.

SURFACE MORPHOLOGY OF $(PE/AU_{NP})_n$ MULTILAYERS

The surface morphologies of $(PE/Au_{NP})_{n\approx 1-4}$ films adsorbed onto Si substrates were examined with an atomic force microscope (AFM) in tapping mode (SPA400, SEIKO). The surfaces of the $(PE/Au_{NP})_n$ films have relatively high root-mean-squared (r.m.s.) surface roughnesses of 3 nm, 5 nm, 6 nm, and 6 nm for $n = 1$, 2, 3 and 4, respectively (see Supplementary Information, Fig. S11). However, in the case of depositing the blocking oxide with 15 nm thickness onto these $(PE/Au_{NP})_n$ films for the fabrication of the non-volatile flash memory devices, the r.m.s. roughness of all the films fell below 2 nm (see Supplementary Information, Fig. S12). The surface morphologies of $(PE/Au_{NP})_{n\approx 1-4}$ films were also investigated by field emission (FE)-SEM (XL30FEG, Philips).

THICKNESS MEASUREMENTS

The thicknesses and refractive indices of the $(PAH/PSS)_n$ films on Si wafers were measured by ellipsometry (Gaertner Scientific, L2W15S830) with 632.8-nm He-Ne laser light. The total thicknesses of the $(PE/Au_{NP})_n$ films were measured from FE-SEM tilted images (that is, the total thicknesses were compensated for the tilt angle of 12.5°).

FABRICATION OF NON-VOLATILE MEMORY DEVICES

All the samples were prepared on p-type Si substrates. Before film deposition, the substrates were cleaned chemically using an aqueous mixture of H_2SO_4:H_2O_2 = 7:3 (vol%), followed by hydrofluoric acid treatment for the removal of SiO_2 and rinsing with deionized water. HfO_2 tunnelling oxide layers of ∼0.9–1.9 nm thickness were then deposited on the substrates using an RF-magnetron sputtering system. The $(PE/Au_{NP})_{n\approx 1-4}$ films for charge-storage media were then formed on the HfO_2-coated Si substrates. For blocking oxide layers, 15-nm-thick HfO_2 layers were deposited using the same method for deposition of the tunnelling oxide. Gate electrodes were fabricated by depositing 100-nm-thick Pt at room temperature by DC magnetron sputtering using pure Ar gas. Gate electrodes with an area of 4.70×10^{-5} cm^2 were patterned using the lift-off process. A copper plate was attached to the backside of Si substrates using silver paint to establish ground contact.

MODIFIED SCANNING NONLINEAR DIELECTRIC MICROSCOPY

The same devices shown in Fig. 2 were used with the exception of the gate electrode. Nanoscale programming/erasing was carried out by placing a conductive AFM tip in direct contact with the $HfO_2/(PE/Au_{NP})_3$ multilayers/HfO_2/Si/Cu plate. The tip was grounded and the bias was applied to the Cu plate contacted with the Si substrate. Sequential erase and program operations were demonstrated by using an AFM.

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Author contributions

J.S.L. and J.C. conceived and designed the experiments, C.L., I.K., J.P. and Y.M.K. performed the experiments, J.S.L and J.C analysed the data, H.S. and J.L. contributed to materials/analysis tools, and F.C. assisted with data interpretation and provided fruitful discussions. J.S.L, J.C. and F.C. co-wrote the paper.

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