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Transistor memory devices with large memory windows, using multi-stacking of densely packed, hydrophobic charge trapping metal nanoparticle array

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Abstract

Organic field-effect transistor (OFET) memories have rapidly evolved from low-cost and flexible electronics with relatively low-memory capacities to memory devices that require high-capacity memory such as smart memory cards or solid-state hard drives. Here, we report the high-capacity OFET memories based on the multilayer stacking of densely packed hydrophobic metal NP layers in place of the traditional transistor memory systems based on a single charge trapping layer. We demonstrated that the memory performances of devices could be significantly enhanced by controlling the adsorption isotherm behavior, multilayer stacking structure and hydrophobicity of the metal NPs. For this study, tetraoctylammonium (TOA)-stabilized Au nanoparticles (TOA-Au_{NPs}) were consecutively layer-by-layer (LbL) assembled with an amine-functionalized poly(amidoamine) dendrimer (PAD). The formed (PAD/TOA-$Au_{NP})_n$ films were used as a multilayer stacked charge trapping layer at the interface between the tunneling dielectric layer and the SiO_2 gate dielectric layer. For a single Au_{NP} layer (i.e. PAD/TOA-$Au_{NP})_1$) with a number density of 1.82×10^{12} cm^{-2}, the memory window of the OFET memory device was measured to be approximately 97 V. The multilayer stacked OFET memory devices prepared with four Au_{NP} layers exhibited excellent programmable memory properties (i.e. a large memory window (ΔV_{th}) exceeding 145 V, a fast switching speed (1 μs), a high program/erase (P/E) current ratio (greater than 10^6) and good electrical reliability) during writing and erasing over a relatively short time scale under an operation voltage of 100 V applied at the gate.

S Online supplementary data available from stacks.iop.org/NANO/25/505604/mmedia

Keywords: OFET, charge trap, multi-stacking, hydrophobic nanoparticles

(Some figures may appear in colour only in the online journal)

[4] These authors equally contributed to this work.

1. Introduction

Recently, numerous attempts have been made toward realizing organic field-effect transistor (OFET) memory devices with a high data storage capacity for use in solid-state hard drives, thereby extending the applications of such devices beyond simple disposable electronics that do not require a high-capacity memory function [1–12]. To this end, various types of OFET memory devices have been designed, including ferroelectric storage [1–3], molecular gate storage [4], polymer electret gate storage [5, 6], protein gate storage [7, 8] and nanofloating gate storage devices [9–11]. Although polymer electret gate storage devices have been reported to exhibit a large memory window (defined as the difference in V_{th} after the application of program/erase bias pulses over a given time period, i.e. $\Delta V_{th} = V_{th,\ ERASE} - V_{th,\ PROGRAM}$) compared to the memory windows displayed by other OFET-type memory devices [5, 6], these transistor memory devices do not permit precise control over the charge trap density and its distribution. The charge trap density and distribution significantly affect the memory characteristics such as the programmed/erased bit distribution, the memory window and the data retention. The recent trend in transistor memory devices has been to store data information at discrete charge trapping sites with well-defined trap levels for improved device control and reliability.

In this view, the nanofloating gate memory devices with metal nanoparticles (NPs) embedded in the gate dielectric are advantageous over other types of OFET memory devices (i.e. ferroelectric, molecular gate and polymer electret gate storage) because they form discrete and stable memory elements [9–11, 13, 14]. Control over the number density and distribution of metal NPs as charge trapping elements can be improved by tuning the NP formation process, for example, by depositing an ultrathin metallic film, implanting ions or depositing materials non-stoichiometrically [9, 11, 15–17]. Recently, several research groups have reported that electrostatically charged metal NPs could be adsorbed onto surfaces using the electrostatic interactions in a solution [18, 19], using microcontact printing methods [20], using blending methods [21] or by embedding metal NPs in block copolymer micelles [13, 14] to prepare discrete charge trapping elements in a nanofloating gate memory. Most of the previous studies of NP-based transistor memory devices, however, have focused on the use of a single charge trapping layer with a relatively small loading of metal NPs. For example, charged metal NPs have been deposited onto oppositely charged substrates using electrostatic interactions. This approach tends to limit the packing density of a NP layer to <30% in the lateral dimension due to the electrostatic repulsion among the same charged NPs [22, 23]. It should also be noted that the rapid dissipation of transferred charges in electrostatically charged metal NPs occurs when the conductive pathways are formed by dipoles, moisture and ions [24].

As another example, Kim *et al* reported the preparation of memory islands with a high density array by block copolymer micelles, including metal NPs. However, their number density was less than approximately $1 \times 10^9\ cm^{-2}$; additionally, the precise and facile control of the charge trap density in block copolymer micelles is not easy to achieve in a large area [25]. Therefore, almost all of the OFET memory (i.e. nanofloating gate memory) devices based on a single NP layer reported to date have had much difficulty achieving high capacity memory despite the aforementioned advantages.

Here, we report the preparation of OFET memory devices with extremely large memory windows using multi-stacked charge trapping layers composed of hydrophobic metal NPs. We demonstrate that the number density of the charge trap sites, which has a decisive effect on the memory performance, can be easily modulated via the adsorption isotherm behavior and bilayer number (i.e. number of stacked layers) of the charge trapping metal NPs. Furthermore, we show that the use of hydrophobic metal NPs instead of electrostatically charged NPs to form discrete charge trap sites is significant for enhancing the memory capacity. For this study, tetraoctylammonium-stabilized Au_{NPs} (i.e. TOA-Au_{NPs}) with a narrow size distribution were synthesized and then consecutively layer-by-layer (LbL) assembled with an amine-functionalized PAD driven by the high affinity between the metal NPs and the amine groups. LbL assembly approaches present a wide range of opportunities for preparing nanocomposite films with a controlled thickness, along with controlled composition and functionality, through complementary interactions (i.e. electrostatic, hydrogen-bonding or covalent interactions) [26–36].

Notably, the hydrophobic TOA-Au_{NPs}, which did not display interparticle electrostatic repulsion, formed densely packed layers on the PAD layer in a nonpolar solvent such as toluene. The resulting charge trap layers could be prepared under an ambient air atmosphere without thermal treatment. This approach has an important advantage in that the number density of hydrophobic metal NPs (i.e. charge trap elements) can be remarkably increased, thereby forming the multi-stacked charge trapping layers (i.e. $(PAD/TOA\text{-}Au_{NP})_n$ multilayers). As the number density of Au_{NPs} in a single-layer structure increased from 1.82×10^{12} to $7.54 \times 10^{12}\ cm^{-2}$, the ΔV_{th} of the Au_{NP}-based nanofloating gate memory devices increased from 97 to 146 V, yielding a P/E current ratio of approximately 10^6 after the application of a program/erase (P/E) bias of $V_G = \pm 100$ V. The reliability of the memory properties was confirmed by measuring the data retention and endurance behaviors. The importance of this work lies in the fact that the memory performances of nanofloating gate memory devices can be notably improved through precise control over the charge trap densities in the vertical dimension as well as in the lateral dimension. Compared with other conventional transistor memory devices, our approach can significantly enhance the memory capacities of transistor memory devices simply by modulating the number of bilayers present and the packing density of charge trap elements.

2. Materials and methods

2.1. Synthesis of TOA-Au_{NPs} and anionic Au_{NPs}

First, 30 mL of an aqueous gold (III) chloride trihydrate ($HAuCl_4 \cdot 3H_2O$, Aldrich) solution (30 mM) were added to a

25 mM solution of tetraoctylammonium bromide ($C_{32}H_{68}BrN$, Aldrich) in 80 mL toluene. In this case, the metal salt was phase-transferred from the aqueous to the toluene phase within a few seconds. A 0.4 M solution of $NaBH_4$ (25 mL, Aldrich) was added to the stirred mixture, which immediately reduced the gold ions. After 30 min, the two phases were separated, and the toluene phase was subsequently washed with 0.1 M H_2SO_4, 0.1 M NaOH and H_2O (three times). After the washing steps, the resulting TOA-Au_{NP} solution dispersed in toluene was used for the LbL deposition, and its diameter was measured to be approximately 6.3 ± 0.7 nm (by a high-resolution transmission electron microscopy (HRTEM) image). The anionic Au_{NPs} (i.e. trisodium citrate ion-stabilized Au_{NPs}) with a diameter of 12 ± 2 nm dispersed in an aqueous solution were synthesized by a citrate reduction method [37]. Briefly, 6 mL of a 1 wt% trisodium citrate dihydrate solution was added to 200 mL water at 70 °C; then, 2 mL of a 1 wt% solution of $HAuCl_4 \cdot 3H_2O$ was successively added to the citrate ion solution. In this case, the mixture turned pink within a few minutes, indicating the formation of anionic gold nanoparticles with carboxylate ion groups. The chemical structures of PAD, TOA-Au_{NP} and anionic Au_{NP} are given in the supporting information, figure S1.

2.2. Build-up of the multilayers

A toluene dispersion of TOA-Au_{NPs} and an ethanol solution of a poly(amidoamine) dendrimer (i.e. $C_{1262}H_{2528}N_{506}O_{252}$ ethylenediamine core, generation 5.0 (PAD), Aldrich) were prepared at concentrations of 1 $mg \cdot mL^{-1}$ and 2 $mg \cdot mL^{-1}$, respectively. Prior to the LbL assembly, the surfaces of the quartz or silicon substrates were treated with an RCA solution ($H_2O/NH_3/H_2O_2$ 5:1:1 *v/v/v*). After RCA treatment, these substrates were dipped into the PAD solution for 10 min, washed twice with ethanol and dried under a gentle air or nitrogen stream. The PAD-coated substrates were dipped into a TOA-Au_{NP} solution for 30 min and were subsequently washed with toluene and dried with air or nitrogen. The dipping cycles were repeated until the desired number of bilayers was obtained.

2.3. Analysis of the multilayers

A quartz crystal microgravimetry (QCM) device (QCM200, SRS) was employed to investigate the mass of the adsorbed PAD and TOA-Au_{NPs}. The mass change (Δm) of the adsorbed PAD and the TOA-Au_{NPs} was calculated from the change in the QCM frequency (ΔF) using the Sauerbrey equation

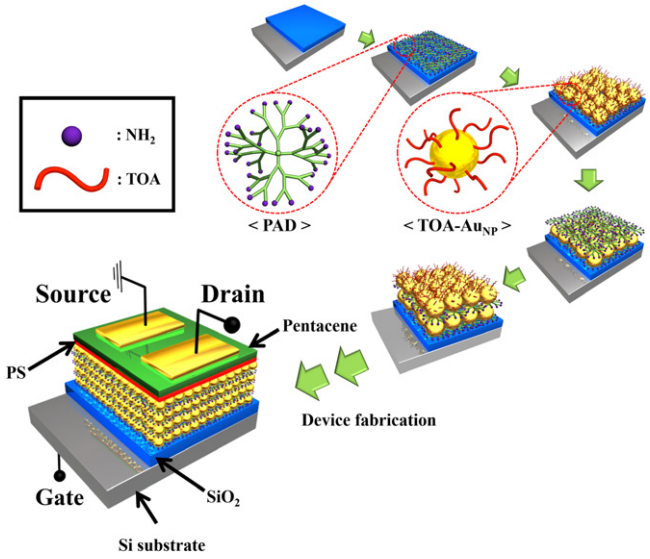
$$\Delta F\,(Hz) = -\frac{2F_0^2}{A\sqrt{\rho_q \mu_q}} \cdot \Delta m$$

where F_0 (5 MHz) is the fundamental resonance frequency of the crystal, A is the electrode area and ρ_q (2.65 $g \cdot cm^{-3}$) and μ_q (2.95×10^{11} $g \cdot cm^{-1} \cdot s^{-2}$) are the density and shear modulus of quartz, respectively. As reported in our previous paper [34], this equation could be simplified as follows

$$\Delta F\,(Hz) = -56.6 \times \Delta m_A,$$

where Δm_A is the mass change per quartz crystal unit area in $\mu g \cdot cm^{-2}$.

The attenuated total reflection (ATR) spectra of the (PAD/TOA-Au_{NP})$_n$ films deposited onto an Au-coated substrate were investigated by Fourier transform infrared spectroscopy (FTIR) (iS10 FT-IR, Thermo Fisher). The sample chamber was purged with N_2 gas for 2 h to remove water and CO_2 before the FTIR measurement. The ATR-FTIR spectra for the (PAD/TOA-Au_{NP})$_n$ films was obtained from 300 scans with an incident angle of 80°.



Scheme 1. Schematic representation of the 3D vertical OFET memory device prepared with a multilayer stacked structure composed of hydrophobic metal NPs.

2.4. Preparation of the OFET memory devices

The heavily doped p-type Si wafer was employed as the gate electrodes, and a thermally grown 300 nm thick SiO_2 was employed as the gate dielectric. The (PAD/TOA-Au_{NP}) multilayers were deposited onto the SiO_2/Si substrate using a LbL assembly process. Polystyrene (PS) (Aldrich, $M_w = 230\,000$) was subsequently spin-coated onto (PAD/TOA-Au_{NP})$_n$ multilayers; then, the film was dried under vacuum. The PS layer with a thickness of approximately 28 nm was used as a tunneling dielectric between the semiconducting channel and the floating gate (i.e. charge trap sites, TOA-Au_{NPs}) [11, 17–20]. In this case, the thickness of the PS layer onto the LbL-assembled (PAD/TOA-Au_{NP})$_1$ multilayers was measured using QCM. That is, the deposition of the PS layer resulted in $-\Delta F$ of 167 ± 1 Hz, which corresponded to about 28 nm thickness (see Sauerbrey equation). Pentacene (Aldrich, no purification) films with a 50 nm thickness were then deposited onto the multilayers at a rate of 0.2 Å sec^{-1} using an organic molecular beam deposition (OMBD) system. The devices were completed by evaporating gold through a shadow mask to define the source and drain

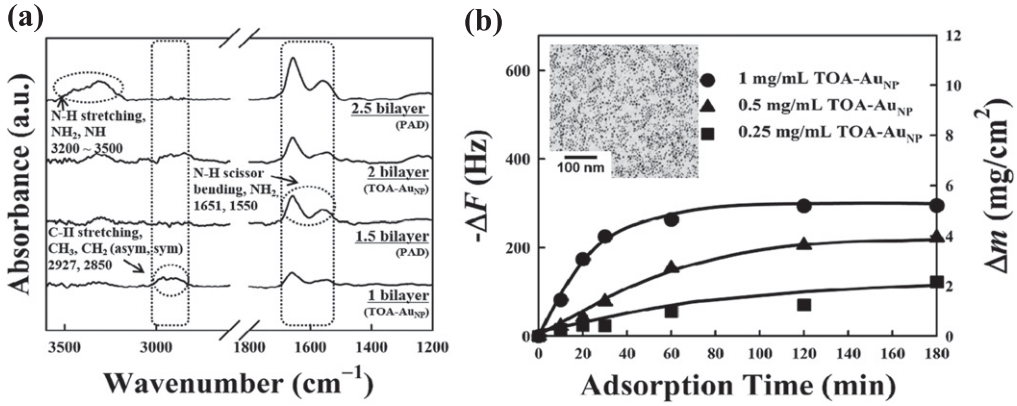


Figure 1. (a) FTIR spectra of the LbL films as a function of the number of $(PAD/TOA\text{-}Au_{NP})_n$ multilayers. The concentrations of the PAD and $TOA\text{-}Au_{NP}$ solutions were adjusted to approximately 2 and 1 $mg \cdot mL^{-1}$, respectively. The materials in parentheses represent the top layers. (b) QCM data of a single $TOA\text{-}Au_{NP}$ layer adsorbed onto the PAD-coated electrode as a function of the deposition time. The inset of (b) shows a HRTEM image of the $TOA\text{-}Au_{NPs}$ (with a diameter of 6.3 ± 0.7 nm) used in our study.

contacts on the pentacene film. The channel length and width were 100 and 1000 μm, respectively. The current-voltage (*I–V*) characteristics of the OFET memory devices were measured at room temperature under ambient conditions in a dark environment using a Keithley 4200 semiconductor parameter analyzer.

3. Results and discussion

For the fabrication of transistor memory devices with multi-stacked charge trapping layers (scheme 1), the hydrophobic $TOA\text{-}Au_{NPs}$ with a diameter of approximately 6.3 ± 0.7 nm were first synthesized in toluene (supporting information, figures S1 and S2) [38, 39]. These NPs were alternately deposited with an alcohol-soluble PAD onto the substrates, including the quartz glass or silicon wafer substrates. Although the TOA stabilizers on the Au_{NP} surfaces had no affinity for the NH_2 groups of the PAD, the quaternary ammonium groups of TOA loosely bound to the Au_{NP} surface could be easily replaced by the $-NH_2$ moieties of the PAD because of the greater affinity [40, 41] between the primary amine groups and the surface of the Au_{NP}.

To confirm this possibility, we investigated the stabilizer-exchange reaction between the TOA stabilizers of the Au_{NPs} and the amine groups of the PAD using FTIR spectroscopy, as shown in figure 1(a). The FTIR spectra of the $TOA\text{-}Au_{NPs}$ and PAD displayed absorption peaks corresponding to the C–H stretching (2850 and 2927 cm^{-1}) of the TOA stabilizers, which included long aliphatic chains, and to the N–H bending vibrations of the PAD (1651 and 1550 cm^{-1}), which included amine groups ($-NH_2$, supporting information, figure S3(a)). The alternating deposition of the PAD and $TOA\text{-}Au_{NP}$ produced inversely correlated changes in the peak intensities of the N–H bending and C–H stretching; that is, as the PAD layer was deposited onto the outermost $TOA\text{-}Au_{NP}$ layer (i.e. $TOA\text{-}Au_{NP}$/PAD/substrate), the C–H stretching peak of the TOA stabilizers at 2850 and 2927 cm^{-1} disappeared, and the N–H bending peak originating from the PAD was intensified (see the FTIR spectrum of the 1.5 bilayer in figure 1(a)).

Here, we exclude the possibility that the disappearance of the C–H stretching peak can be caused by the mere accumulation of the PAD onto the outermost $TOA\text{-}Au_{NP}$ layer rather than the ligand exchange between the TOA ligands and primary amine groups of the PAD. More specifically, the adsorption of $TOA\text{-}Au_{NPs}$ with a diameter size of 6.3 ± 0.7 nm onto the outermost PAD layer (i.e. transition from the 1.5 to 2 bilayer) does not decrease the peak intensities by the N–H stretching and bending (at 3200, 1651, 1550 cm^{-1}) of the PAD because $TOA\text{-}Au_{NPs}$ have no absorption peak at 3200, 1651 and 1550 cm^{-1}. Similarly, the adsorption of the PAD layer onto the outermost $TOA\text{-}Au_{NPs}$ has no detectable effect on the absorption peaks of TOA ligands due to the above-mentioned reason. If the successive LbL assembly process is not based on the ligand exchange reaction, the absorption peak of TOA stabilizers should be continuously increased with increasing the bilayer number because the PAD layer has no absorbance peak in the range of 2927 and 2850 cm^{-1}. However, in our study, the absorption peak of TOA stabilizers bound to the surface of Au_{NPs} almost disappeared when the PAD layer was deposited onto the outermost $TOA\text{-}Au_{NP}$ layer. Additionally, we did not observe the growth of TOA ligands despite an increase of the bilayer number. These results imply that TOA stabilizers can be detected in only the outermost $TOA\text{-}Au_{NP}$ layer rather than the buried Au_{NP} layers.

Furthermore, we investigated the change in the peak intensities of the $TOA\text{-}Au_{NP}$ and the PAD as a function of the deposition time of the PAD (supporting information, figure S3(b)). In this case, the C-H stretching peak (at 2850 and 2927 cm^{-1}) originating from the TOA stabilizer gradually disappeared; on the other hand, the N-H bending vibration peak of the PAD at 1651 and 1550 cm^{-1} is more intensified with increasing the deposition time of the PAD adsorbed onto the outermost $TOA\text{-}Au_{NP}$-coated substrate (i.e. $TOA\text{-}Au_{NP}$/PAD/substrate) from 0 to 2 h. These results clearly indicated that a multilayered stack of charge trapping Au_{NP} layers could

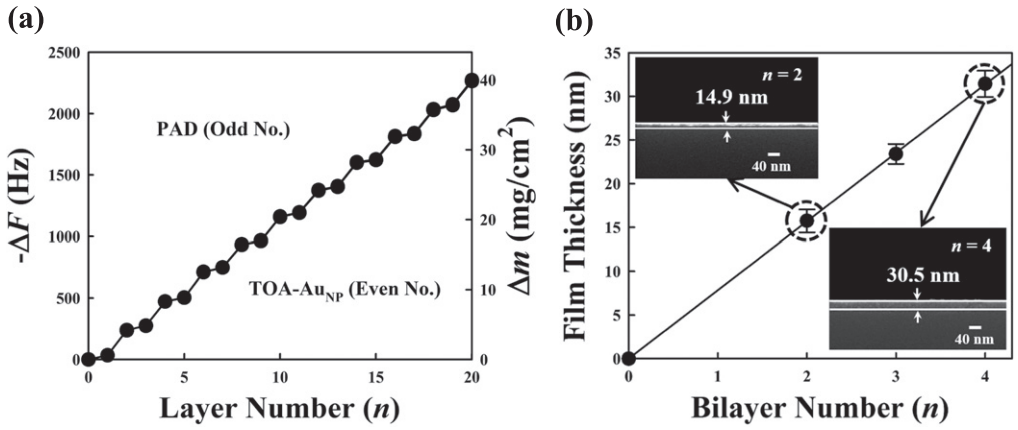


Figure 2. (a) QCM data for the (PAD/TOA-Au$_{NP}$)$_n$ as a function of the layer number. (b) Total film thickness values of the (PAD/TOA-Au$_{NP}$)$_4$ multilayers as a function of the bilayer number. The inset of (b) shows the cross-sectional images of the (PAD/TOA-Au$_{NP}$)$_{n=2 \text{ and } 4}$ multilayers.

be prepared using successive stabilizer-exchange reactions between the PAD and the TOA stabilizers of the Au$_{NPs}$.

On the basis of these results, we investigated the adsorption isotherm behavior and the number density of adsorbed TOA-Au$_{NPs}$ per layer as a function of the adsorption time and concentration of TOA-Au$_{NPs}$ using QCM. Figure 1(b) shows the frequency changes, $-\Delta F$, and the mass changes in the adsorbed TOA-Au$_{NPs}$ that resulted from the increased deposition time. The inset of figure 1(b) shows a HRTEM image of the TOA-Au$_{NPs}$, 6.3 ± 0.7 nm in diameter, used in our study. The mass changes were calculated from the frequency changes ($-\Delta F$) of the TOA-Au$_{NPs}$ adsorbed onto the PAD-coated QCM electrode. As the concentration of the TOA-Au$_{NP}$ solution increased from 0.25 to 1 mg $\cdot$ mL^{-1}, the adsorption time required to reach a saturated amount of TOA-Au$_{NPs}$ rapidly decreased. In the case of a TOA-Au$_{NP}$ solution with a concentration of 1 mg $\cdot$ mL^{-1}, the quantities of TOA-Au$_{NPs}$ adsorbed onto the PAD layer nearly reached a plateau after 30 min, which resulted in a $-\Delta F$ of 225 ± 5 Hz (Δm of 3975 ng $\cdot$ cm^{-2}). Additionally, these phenomena imply that the use of a TOA-Au$_{NP}$ concentration higher than 1 mg $\cdot$ mL^{-1} can shorten the adsorption time for a saturated amount of TOA-Au$_{NPs}$. Given that the diameter and density of the TOA-Au$_{NPs}$ used were approximately 6 nm and 19.3 g $\cdot$ cm^{-3}, respectively, the number density of the TOA-Au$_{NPs}$ in a single layer was calculated to be 1.82×10^{12} cm^{-2} after 30 min (i.e. the Δm of 3975 ng $\cdot$ cm^{-2} measured from QCM were divided by the density of Au NPs and the volume of single Au NPs), which corresponded to a 2D packing density of approximately 52%. The number of TOA-Au$_{NPs}$ adsorbed onto the PAD layer was also counted out using a SEM image because it was assumed that the mass density of TOA-Au$_{NPs}$ in the QCM analysis was identical to that of bulk Au. In the case of the TOA-Au$_{NPs}$ deposition for 30 min, the number density of the TOA-Au$_{NPs}$ was calculated to be approximately 1.32×10^{12} cm^{-2} (i.e. a 2D packing density of about 42%).

Furthermore, the growth of the multilayer Au$_{NP}$ structure was quantitatively monitored using QCM (figure 2(a)). For the processing time efficiency, the deposition time for the adsorption of 1 mg $\cdot$ mL^{-1} TOA-Au$_{NPs}$ was determined to be 30 min. The alternating deposition of the PAD and the TOA-Au$_{NP}$ layers resulted in the regular growth of $-\Delta F$ as a function of the layer, indicating that the quantity of TOA-Au$_{NPs}$ adsorbed per layer was consistent. The total loading amount and the number density of TOA-Au$_{NPs}$ within the (PAD/TOA-Au$_{NP}$)$_4$ multilayers were calculated to be approximately 1.64×10^4 ng $\cdot$ cm^{-2} and 7.54×10^{12} cm^{-2}, respectively. The formation of the (PAD/TOA-Au$_{NP}$)$_4$ multilayers was further characterized by collecting cross-sectional SEM images. The total film thickness values of the (PAD/TOA-Au$_{NP}$)$_n$ multilayers were approximately 14.9 nm for $n = 2$, 23.4 nm for $n = 3$ and 30.5 nm for $n = 4$ (figure 2(b)). We also confirmed the vertical growth of (PAD/TOA-Au$_{NP}$)$_n$ multilayers using UV–vis spectroscopy (supporting information, figure S4). The surfaces of the (PAD/TOA-Au$_{NP}$)$_{n=1-4}$ multilayer films were highly uniform and displayed an extremely low root-mean-squared (RMS) surface roughness of less than 1.5 nm (supporting information, figure S5). The TOA-Au$_{NPs}$ that were adsorbed onto the PAD layers were well dispersed and isolated in the lateral dimension due to the presence of the bulky TOA stabilizers bound to the surfaces of the Au$_{NP}$, despite a lack of an electrostatic repulsion among the neighboring Au$_{NPs}$. The PAD layer inserted between the Au$_{NP}$ layers allowed individual Au$_{NPs}$ to operate as isolated charge trap elements in the vertical and lateral dimensions. The (PAD/TOA-Au$_{NP}$)$_n$ multilayers have the insulating property that shows a high sheet resistance (>10^8 $\Omega \cdot \square^{-1}$) and an extremely low electrical conductivity (not measured by a four-point probe) due to the insulating PAD materials and hydrophobic TOA ligands adsorbed onto the discrete Au$_{NPs}$.

Based on these results, the LbL-assembled (PAD/TOA-Au$_{NP}$)$_n$ multilayers were utilized as a floating gate of the nanofloating gate memory devices (scheme 1). First, the output characteristics measured from single Au$_{NP}$ layer-based devices exhibited typical p-channel OFET behavior, indicating that the insertion of a metal NP layer between the SiO_2 blocking and PS tunneling dielectrics of about 28 nm thickness did not affect the OFET performance (figure 3(a))

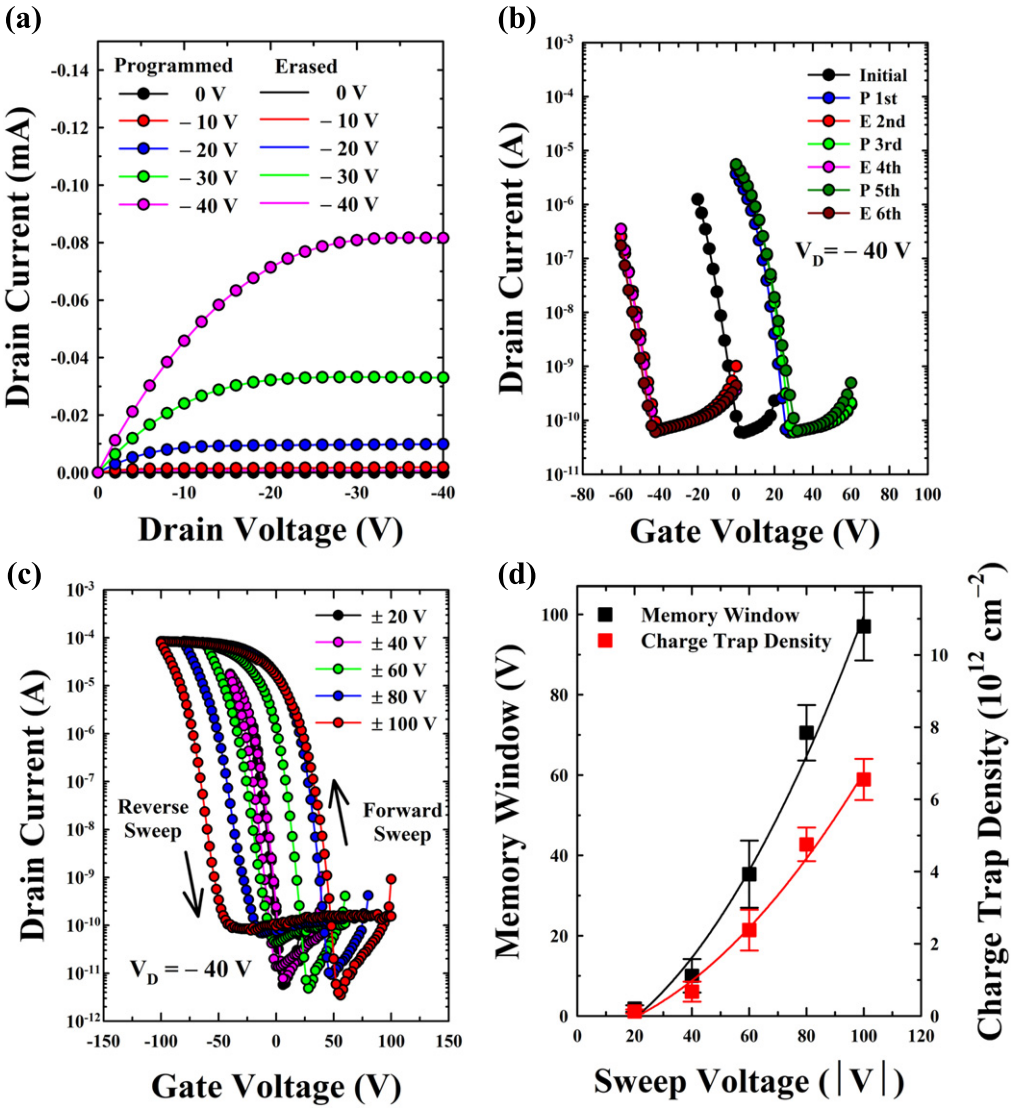


Figure 3. (a) Output characteristics of the 3D vertical OFET memory devices prepared with $(PAD/TOA\text{-}Au_{NP})_1$ charge storage layers. The curves were obtained after applying $V_{G,\ PROGRAM} = +100$ V for 1 s and $V_{G,\ ERASE} = -100$ V for 1 s. (b) Shifts in the transfer curves of the OFET memory devices prepared with $(PAD/TOA\text{-}Au_{NP})_1$ charge storage layers ($V_{G,\ PROGRAM} = +100$ V for 1 s and $V_{G,\ ERASE} = -100$ V for 1 s). (c) Memory hysteresis behavior of the OFET memory devices prepared with a $(PAD/TOA\text{-}Au_{NP})_1$ charge storage layer as a function of the V_G sweep range from ±20 V (forward sweep: +20 V → −20 V; reverse sweep: −20 V → +20 V) to ±100 V (forward sweep: +100 V → −100 V; reverse sweep: −100 V → +100 V). (d) Memory window and charge trap density versus the V_G sweep range.

[9, 11, 17, 42]. The $(PAD/TOA\text{-}Au_{NP})_1$ device exhibited a saturation field-effect mobility (μ_{FET}) of 0.23 $cm^2 \cdot V^{-1} \cdot s^{-1}$, a threshold voltage ($V_{th}$) of 7.60 V and an ON/OFF current ratio of $\sim 10^5$, all of which were comparable to the values reported previously for pentacene transistors [9, 14, 42]. A substantial shift in V_{th} was observed upon the application of a gate voltage ($V_G = +100$ V (program, P) or −100 V (erase, E)) over a relatively short time (1 s), as shown in figure 3(b). That is, as the device was subjected to a programmed V_G of +100 V, the hole carriers were injected from the $TOA\text{-}Au_{NPs}$ into the pentacene layer (or the electron carriers were injected from the pentacene layer into the $TOA\text{-}Au_{NPs}$). These phenomena induced high electric conductivity (i.e. ON state) and a positive V_{th} shift. Reversely, the application of a negative gate bias for erase (−100 V) resulted in the transfer of the hole carriers from the pentacene to the $TOA\text{-}Au_{NPs}$. The trapped hole charges within the $TOA\text{-}Au_{NPs}$ built up an internal electric field that partially screened the external electric field (V_G), which resultantly induced the low electric conductivity (OFF state), followed by a negative V_{th} shift. This shift in the transfer curve was attributed to the charges trapped within the Au_{NPs}, as already reported by other research groups (supporting information, figure S6) [11, 17–20]. In addition, it was reported that the memory effects of proton migration in the SiO_2 can be influenced by the presence of residual water molecules and mobile ions [43, 44]. However, considering that the floating gate dielectric layers (i.e. $PAD/TOA\text{-}Au_{NP}$ multilayers) of the OFET memory devices in our study were prepared using successive LbL assembly in an organic solvent media, such as toluene (for hydrophobic $TOA\text{-}Au_{NP}$) and ethanol (for PAD) instead of an aqueous solvent, the proton

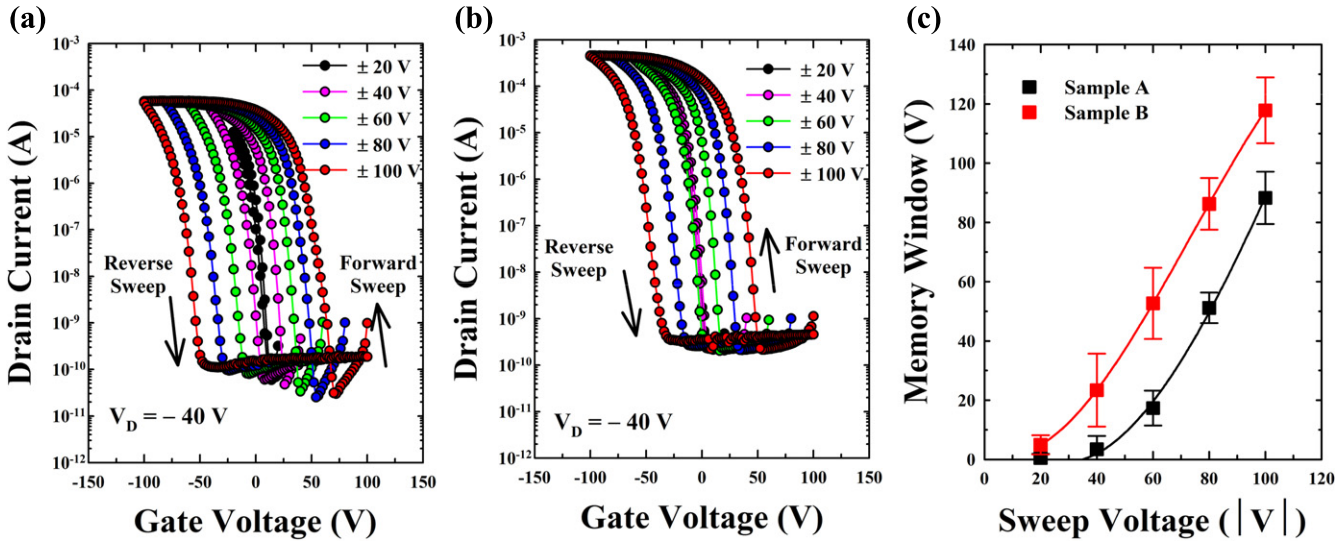


Figure 4. Memory hysteresis behavior of the OFET memory devices prepared with (a) $(PAD/TOA\text{-}Au_{NP})_2$ and (b) $[(PAD/TOA\text{-}Au_{NP})_1/(PAD/PAA)_3/(PAD/TOA\text{-}Au_{NP})_1]$ charge storage layers as a function of the V_G sweep range from ±20 V to ±100 V. (c) Memory window of the OFET memory devices prepared with $[(PAD/TOA\text{-}Au_{NP})_1/(PAD/PAA)_3/(PAD/TOA\text{-}Au_{NP})_1]$ (Sample A) and $(PAD/TOA\text{-}Au_{NP})_2$ (Sample B) charge storage layers as a function of the V_G sweep range.

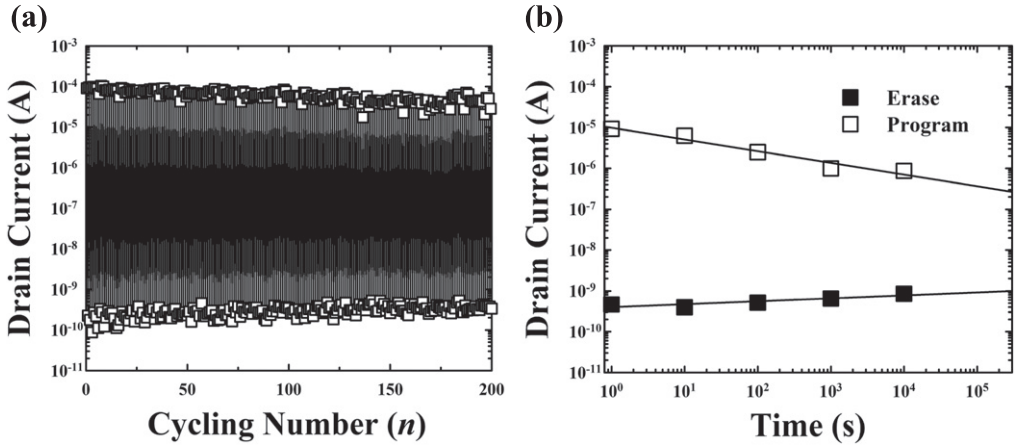


Figure 5. (a) Cycling and (b) retention time tests for the OFET memory devices prepared with $(PAD/TOA\text{-}Au_{NP})_2$ charge storage layers.

migration-induced memory effects are minimized in our devices.

The memory window (ΔV_{th}) of the devices depended strongly on the number of trapped charges present in the Au_{NPs}, which relied on the magnitude of the applied gate voltages. As the gate voltage (V_G) sweep range was increased from ± 20 V (forward sweep: +20 V → −20 V; reverse sweep: −20 V → +20 V) to ±100 V (forward sweep: +100 V → −100 V; reverse sweep: −100 V → +100 V), the memory window of the $(PAD/TOA\text{-}Au_{NP})_1$-based device increased dramatically from 2 to 97 V (figures 3(c) and (d)). Given that the number of trap charges could be calculated using the equation $\Delta n = C_i \cdot \Delta V_{th}/e$ (where C_i and e are the specific capacitance of the gate dielectric (10.8 $nF \cdot cm^{-2}$) and the element charge, respectively) [45], the total number of trapped charges in the $(PAD/TOA\text{-}Au_{NP})_1$-based device for the V_G sweep range of ±100 V was calculated to be approximately 6.55×10^{12} cm^{-2}. A total of 3.6 charge carriers were, therefore, trapped in each Au_{NP}.

Leong *et al* reported that the Au_{NPs} synthesized within the poly(styrene)-*block*-4-poly(4-vinylpyridine) (i.e. PS-*b*-P4VP) block copolymer micelles (BCMs) could be used as charge storage elements for the OFET memory devices [13]. These devices exhibited a ΔV_{th} of 10 V after the application of $V_{G,\ ERASE} = -30$ V for 1 s and $V_{G,\ PROGRAM} = +100$ V for 30 s. The OFET memory devices based on Ag_{NP}- and Pt_{NP}-incorporated BCMs were reported by Chen *et al* [14]. The memory windows of the Ag_{NP}- and Pt_{NP}-incorporated BCM devices were found to be approximately 19 and 27 V, respectively. Although the metal NP-embedded BCMs permit the formation of discrete charge trap elements, the control over the number density of charge trap elements and the ability to enhance the memory capacity has been highly limited. These results, in view of the memory capacity, suggested that our LbL-assembly approach using multilayers of hydrophobic metal NPs was more effective than the block copolymer micelle method that yields a relatively low quantity of charge trap sites due to the formation of a large vacant

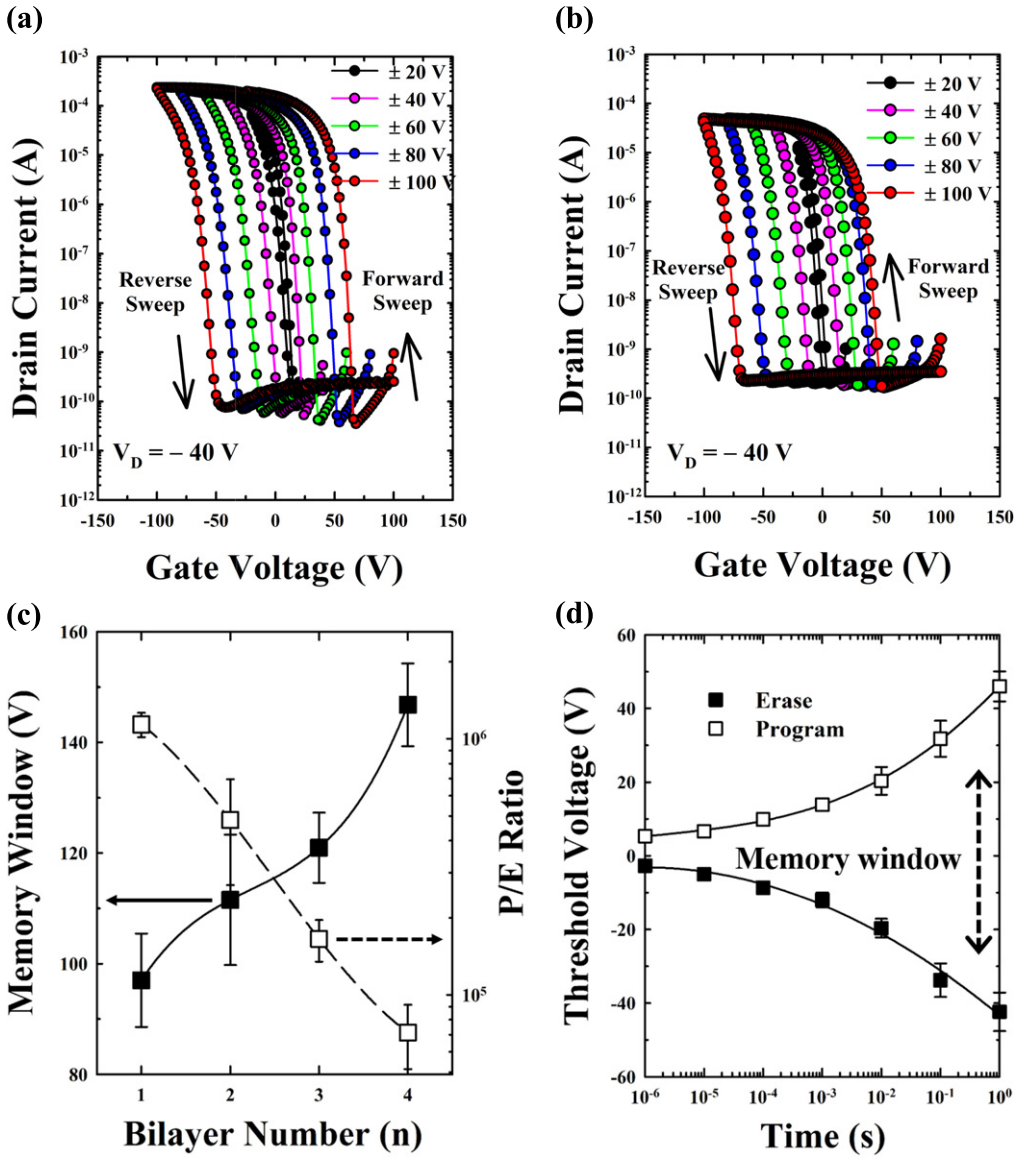


Figure 6. Memory hysteresis behavior of the OFET memory devices prepared with (a) (PAD/TOA-Au_{NP})$_3$ and (b) (PAD/TOA-Au_{NP})$_4$ charge storage layers as a function of the V_G sweep range. (c) Memory window and the P/E ratio for the OFET memory devices as a function of the bilayer number (n) (i.e. (PAD/TOA-Au_{NP})$_n$ for $n = 1$–4). (d) P/E speeds of the OFET memory devices.

space between the neighboring micelles, as well as the single-layer structure of the micelle array.

On the basis of these results, we investigated the memory window of the OFET memory devices prepared with multi-structured charge storage layers. First, OFET memory devices bearing two stacked charge trapping layers (i.e. (PAD/TOA-Au_{NP})$_2$) were prepared (figure 4(a)). The memory window of the device was increased from 3 to 118 V as the V_G sweep range was increased from ±20 to ±100 V. This window was much larger than that of a device prepared with a single charge trapping layer under the same sweep range conditions due to an increase in the charge trapping sites along the vertical dimension. For comparison, the insulating multilayers (i.e. [PAD/poly(acrylic acid) (PAA)]$_3$) with a thickness of approximately 6 nm were inserted to achieve a more distinct separation between the top and bottom charge trapping Au_{NP} layers (i.e. (PAD/TOA-Au_{NP})$_1$/(PAD/PAA)$_3$/(PAD/TOA-Au_{NP})$_1$ multilayers), and their thickness almost corresponded to the diameter of TOA-Au_{NP}. However, the PAD and (PAD/PAA)$_3$ layers did not clearly separate the respective Au NP layers due to the infiltration phenomena of Au NPs into multilayers, as shown in the cross-sectional TEM images (supporting information, figure S7). It has been reported that the organic/inorganic NP nanocomposite multilayers prepared from the dipping-based LbL assembly have a blended or disordered internal structure instead of a well-ordered internal structure [41, 46, 47].

Figure 4(b) shows the memory hysteresis behavior of the devices prepared with insulating separation layers. The memory window was smaller than that of the device (i.e. the (PAD/TOA-Au_{NP})$_2$ multilayered device) prepared without insulating separation layers (figure 4(c)). The insertion of additional insulating layers blocked the charge trapping in the bottom Au_{NP} layer due to the exponential decay of the

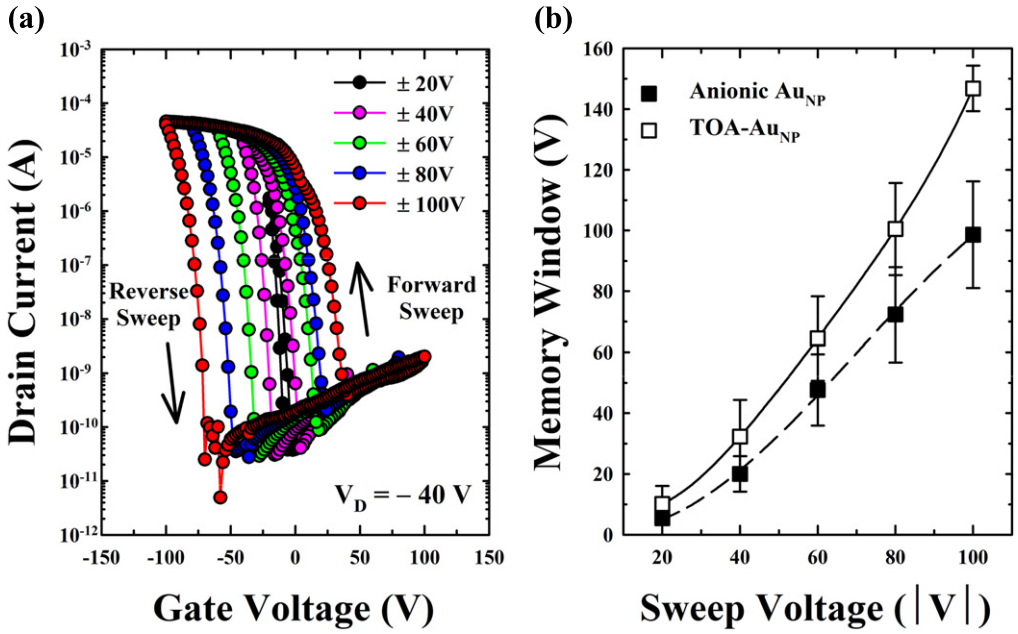


Figure 7. (a) Memory hysteresis behavior of the OFET memory devices prepared with (cationic NH_3^+-PAD/anionic $Au_{NP})_4$ charge storage layers as a function of the V_G sweep range from ±20 V to ±100 V. The solution pH of the cationic NH_3^+-PAD and of the anionic Au_{NP} was adjusted to pH 6. The total number density of anionic Au_{NPs} within the multilayers was measured to be about 5.56×10^{11} cm^{-2}. (b) Memory windows of the OFET memory devices prepared with (PAD/TOA-$Au_{NP})_4$ and (cationic NH_3^+-PAD/anionic $Au_{NP})_4$ charge storage layers, according to the V_G sweep range from ±20 to ±100 V.

tunneling probability as the insulating layer thickness increased. The memory characteristics of the OFET memory device prepared with the inserted insulating multilayers depended strongly on the top Au_{NP} layer rather than on the bottom Au_{NP} layer. As a result, the memory window of this device ($\Delta V_{th} \sim 95$ V) was similar to that of the OFET memory device ($\Delta V_{th} \sim 97$ V) prepared with a single charge storage layer (i.e. PAD/TOA-$Au_{NP})_1$ device). These results revealed that the multilayered stacks of the charge storage elements without additional insertion of insulating layers significantly improved the memory performance.

We tested the retention time and cycling performances of the (PAD/TOA-$Au_{NP})_2$-based OFET memory devices to confirm the long-term stability of the (PAD/TOA-$Au_{NP})_2$ charge storage device. In these cases, the P/E current states were kept continuously stable during the repeated cycling tests of approximately 200 cycles with a pulse width of 1 s (figure 5(a)) and a test period of 10^4 s in air (figure 5(b)). Although the PS layer employed as a tunneling dielectric layer in our study may also be used as a chargeable gate dielectric material, the OFET memory devices composed of a PS and PAD layer onto SiO_2 without a TOA-Au_{NP} layer exhibited poor retention stability, implying that these layers (i.e. PS and PAD) have only shallow charge trap sites (supporting information, figure S8).

We further increased the number of bilayers (n) and examined the properties of the devices (i.e. (PAD/TOA-$Au_{NP})_n$). Figures 6(a) and (b) show the representative memory hysteresis behaviors in the 3- and 4-bilayer memory devices, respectively. The increase in the bilayer number significantly enhanced the memory window due to an increase in the Au_{NP} charge trap sites along the vertical dimension. For example, the memory window of the 4-bilayered device was measured to be 146 V, accompanied by a P/E current ratio of $\sim 10^5$ for a V_G sweep range of ±100 V (figure 6(c)). The increased dielectric multilayer thickness (i.e. an increase in the bilayer number) slightly decreased the P/E current ratio due to a reduction in the electric field, as shown in figure 6(c). The P/E speeds of the devices were investigated by applying program (P) voltage of +100 V and erase (E) voltages of −100 V to the gate electrode at pulse widths that varied from 1 to 10^{-6} s (figure 6(d)). Although the shift in V_{th} decreased gradually as the P/E switching speed decreased, a reasonable shift in V_{th} was obtained by applying a bias pulse longer than 1 μs. That is, a switching time longer than at least 1 μs is typically required to fully switch on or off the memory devices.

It should be noted that our approach using multilayer stacking can be applied to the transistor memory devices based on electrostatically charged Au_{NPs} (figure 7). The electrostatic LbL-assembled (NH_3^+-PAD/anionic $Au_{NP})_4$ layers exhibited a memory window of approximately 100 V for a V_G sweep range of ±100 V. The memory window of the device prepared with electrostatic LbL-assembled (NH_3^+-PAD/anionic $Au_{NP})_4$ layers was found to be lower than that of the (PAD/TOA-$Au_{NP})_4$-based device, which is mainly due to the possibility that the rapid dissipation of transferred charges through electrostatically charged (or highly hydrophilic) ligands occurs via the conductive pathways formed by dipoles, residual moisture and ions [24]. However, in spite of these electrostatically charged multilayers, the memory window of approximately 100 V has never previously been

accomplished in conventional nanofloating gate memory devices with a single-layer structure. Overall, our results show that the use of a hydrophobic metal NP array (i.e. charge trap elements) with a dense packing structure in the lateral dimension and a multilayer structure are essential for fabricating high-performance transistor memory devices.

4. Conclusions

We demonstrated that nanofloating gate memory devices based on multilayer stacks of densely packed hydrophobic metal NP arrays could significantly enhance their memory capacity due to a remarkable increase in the charge trap elements with hydrophobic properties. We also demonstrated that the number density of charge trap sites could be easily controlled and precisely predicted based on the adsorption isotherm behavior of the metal NPs as discrete charge trap elements. Notably, the use of a hydrophobic metal NP as a charge trap element synergistically improved the memory performance. Consequently, the $(PAD/TOA\text{-}Au_{NP})_n$ multilayer stacked devices exhibited an extremely large memory window exceeding 145 V and a high P/E current ratio of $\sim 10^6$. To our knowledge, this large memory window demonstrated in our study has not been previously obtained from conventional transistor memory devices. Our approach, which involved multilayer stacks of hydrophobic NPs, could provide a basis for the development of disposable but high-capacity OFET memory devices.

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Supporting information

The FTIR spectra and transmission curves of the films; the SEM, TEM and AFM images of the multilayers; and the *I-V* curves of multilayer devices are shown in the supporting information.

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