Organic Field-Effect Transistor Memory Devices Using Discrete Ferritin Nanoparticle-Based Gate Dielectrics

Beom Joon Kim, Yongmin Ko, Jeong Ho Cho, and Jinhan Cho**

Organic field-effect transistor (OFET) memory devices made using highly stable iron-storage protein nanoparticle (NP) multilayers and pentacene semiconductor materials are introduced. These transistor memory devices have nonvolatile memory properties that cause reversible shifts in the threshold voltage (V_{th}) as a result of charge trapping and detrapping in the protein NP (i.e., the ferritin NP with a ferrihydrite phosphate core) gate dielectric layers rather than the metallic NP layers employed in conventional OFET memory devices. The protein NP-based OFET memory devices exhibit good programmable memory properties, namely, large memory window ΔV_{th} (greater than 20 V), a fast switching speed (10 μs), high ON/OFF current ratio (above 10^4), and good electrical reliability. The memory performance of the devices is significantly enhanced by molecular-level manipulation of the protein NP layers, and various biomaterials with heme Fe^{III}/Fe^{II} redox couples similar to a ferrihydrite phosphate core are also employed as charge storage dielectrics. Furthermore, when these protein NP multilayers are deposited onto poly(ethylene naphthalate) substrates coated with an indium tin oxide gate electrode and a 50-nm-thick high-k Al_2O_3 gate dielectric layer, the approach is effectively extended to flexible protein transistor memory devices that have good electrical performance within a range of low operating voltages (<10 V) and reliable mechanical bending stability.

1. Introduction

Organic nonvolatile memory devices have recently attracted significant attention because of the huge demand for flexible, printable, and disposable electronics. Many attempts have been made to realize organic memory devices of varying types, such as two-terminal organic (or organic–inorganic) bistable capacitor devices (i.e., resistive switching or charge-trap flash memory devices)[1–4] or transistor-type devices (i.e., organic field-effect transistor (OFET) memory devices).[5–18] Among the organic nonvolatile memory device configurations, OFETs with nonvolatile memory are promising candidates for future applications because of their nondestructive readout, low power consumption, and direct integrated circuit architectural compatibility. OFET-type memory devices can be further classified based on their operating mechanisms as ferroelectric storage,[5–7] molecular gate storage,[8] polymer electret gate storage,[9] or nanofloating gate storage[11–14] devices. Although several types of OFET memory devices and various synthesized organic (or organic–inorganic) hybrid materials for gate dielectrics have been introduced in an effort to realize high-performance devices, one of the most critical challenges has been the facile increase of memory density using stable and discrete charge storage elements.

Toward the fabrication of discrete and stable memory elements, significant attention has been focused on OFET memory devices that use metal nanoparticles (NPs) or metal NP-incorporated block-copolymer micelles (BCMs) as discrete charge storage elements to reduce the charge loss from defects in the dielectrics and provide good electron

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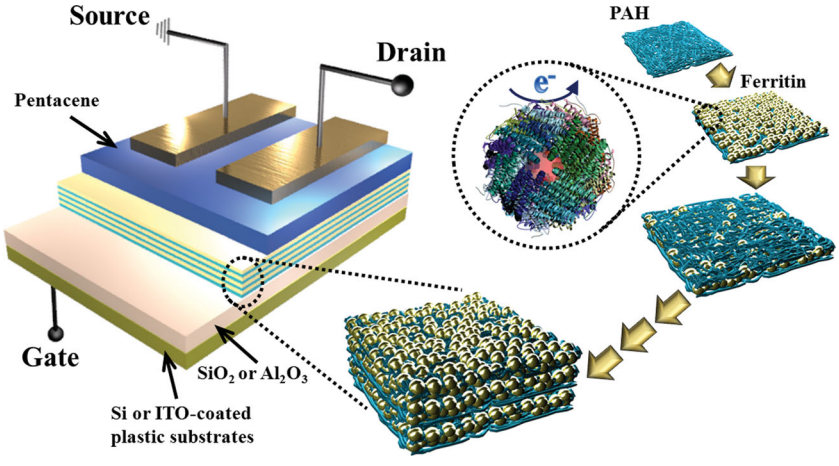
trapping capabilities.[11–14] Medalsy *et al.* also reported that protein-encapsulated silicon NPs can be used as a discrete memory unit.[19] However, the proteins used in their study were employed as a stabilizer for the preparation of isolated Si NPs, and the memory function for electron charging and releasing was introduced by silicon NPs. Additionally, Ohara et al. prepared nanodot floating-gate-type metal oxide semiconductor (MOS) capacitors and a MOS field-effect transistor (MOSFET) memory device using cobalt NP-accommodated ferritin.[20] However, the ferritins used in their study were employed to prevent the agglomeration of Co NPs during deposition; the ferritin shell was then removed by UV irradiation in an ozone atmosphere. As a result, the memory characteristics of their MOS or MOSFET devices originated entirely from the discrete Co NPs. Although memory devices using metal NPs, BCMs, or protein-encapsulated metal NPs are advantageous over conventional nanofloating gate memory devices because of their discrete charge storage elements, these devices are mainly based on single-layered charge storage elements and, consequently, impose a constraint on vertical addition of charge storage layers for enhancing the memory capacity. Therefore, it is critical to improve the architecture for charge storage elements and, further, to develop a simple and versatile process for increasing the number density of charge storage elements in the vertical dimension.

Herein, we report OFET memory devices based on multistructured ferritin NP layers that permit discrete charge trapping and facile control over the quantity of protein NPs adsorbed onto a substrate. For this study, we used a ferritin NP that is a highly stable iron-storing protein with an outer diameter of 12 nm and a shell thickness of 2 nm[21,22] as a charge-storing gate dielectric in a pentacene field-effect transistor memory device. Ferritin multilayer films were prepared by the successive layer-by-layer (LbL) deposition of cationic poly(allylamine hydrochloride) (PAH) and anionic ferritin NPs onto 200-nm-thick SiO_2 insulator-coated or 50-nm-thick Al_2O_3-coated plastic substrates at room temperature (**Scheme 1**). It should be noted that the LbL assembly method is useful for preparing functional films with tailored electrical properties and layer thicknesses on a variety of substrates.[23–36] Our approach demonstrates that protein NPs with redox sites can be effectively employed as discrete gate dielectrics with deep charge trap states in place of metal NPs for use in transistor memory devices. Furthermore, we demonstrate that the charge trap density can be significantly increased in the vertical dimension by using this process and the resultant performance parameters of the device, such as the memory window and program/erase current ratio, can be adjusted according to the bilayer number of the charge storage layer. It should be noted here that conventional OFET memory devices have been based on the use of a single charge storage layer (e.g., metal NPs, BCMs, and protein-encapsulated metal NPs), which makes it difficult to control device performance. Even though proteins were used as charge storage gate dielectrics in the present study, these devices have a large memory window (>20 V) and a high program/erase (P/E, or ON/OFF) current ratio (>10^4). Reliable memory properties were confirmed by measuring the data retention and endurance. This approach can easily be extended to flexible transistor memory devices with low operating voltages by using high-k Al_2O_3 gate dielectrics in place of SiO_2. The importance of our work lies in the potential use of proteins as charge storage gate dielectrics for transistor memory devices and the potential to increase the memory density through the multistacking of charge storage layers in the vertical dimension.

2. Results and Discussion

First, we deposited poly(allylamine hydrochloride) (PAH)/ferritin NP multilayers onto substrates by using electrostatic LbL assembly at pH 9.0 as previously reported.[35] Ferritin multilayers were quantitatively analyzed by quartz crystal microgravimetry (QCM), which determines the amount of cationic PAH (pK_a approximately equal to 9)[36] and the number of anionic ferritin NPs (isoelectric point, p*I*, approximately equal to 4.5).[37] The changes in mass were calculated from the changes in frequency by using the Sauerbrey equation (see Experimental Section). These QCM frequency (or mass) changes suggest that regular multilayer film growth occurred under conditions in which PAH and ferritin NPs were LbL-assembled from a deposition solution (**Figure 1**a). The alternate deposition of PAH and ferritin NPs resulted in a $-\Delta F$ of 22 ± 3 (Δm of 392 ± 21 ng cm^{-2}) and 61 ± 3 Hz (Δm of 1085 ± 21 ng cm^{-2}) for these layers, respectively. In this case, the total PAH/ferritin multilayer film thickness increased linearly from 58 ± 3 to 231 ± 5 nm with a corresponding increase from 10 to 40 bilayers (Figure 1b). The measured thicknesses did not correspond exactly to the ideal film thickness, assuming a 12-nm-thick ferritin layer, adsorbed PAH layer thickness, and bilayer number, because of insufficient



Scheme 1. Schematic representation of the OFET memory device with LbL-assembled (PAH/ferritin NP)$_n$ multilayered gate dielectrics.

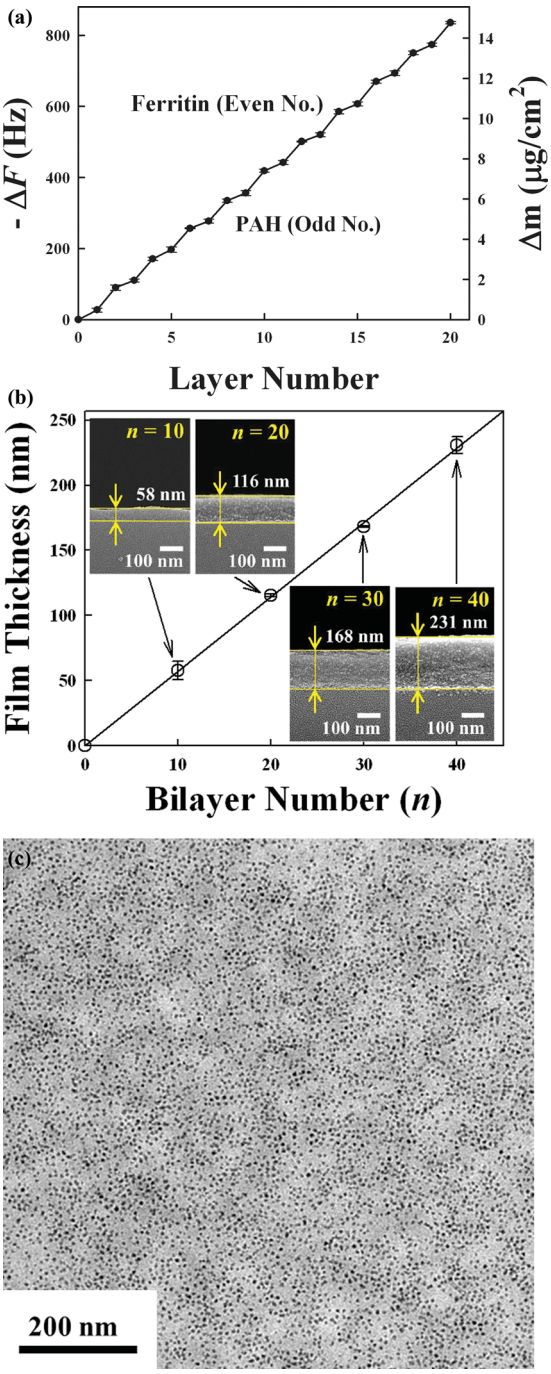


Figure 1. a) QCM data for $(PAH/ferritin\ NP)_n$ as a function of layer number. b)Film thicknesses of the $(PAH/ferritin\ NP)_n$ multilayers, measured from cross-sectional scanning electron microscopy images obtained after drying under vacuum. c) High-resolution (HR) TEM image of a single ferritin NP layer adsorbed onto a PAH-coated TEM grid.

ferritin surface coverage resulting from electrostatic repulsion between species with an identical charge. Transmission electron microscopy (TEM) images of a single ferritin layer formed on a PAH-coated TEM grid support this explanation (Figure 1c). The images show that the number density of ferritin molecules per layer was 1.8×10^{11} cm^{-2}.

Several research groups have demonstrated that the presence of a ferrihydrite phosphate core in ferritin produces electrochemical redox behavior in a phosphate-buffered saline (PBS) solution because of the reversible charge trapping/release of Fe^{III}/Fe^{II} pairs.[35,38,39] Based on these previous results, we investigated the electrochemical redox behavior of PAH/ferritin multilayer-deposited indium tin oxide (ITO) glass by using cyclic voltammetry (CV) in PBS at pH 7. In this case, the multilayers exhibited typical redox peaks at –0.14 (for oxidation) and –0.28 V (for reduction), and the increased scan rates resulted in higher intensities of the redox peak (Supporting Information (SI), Figure S1). However, we observed no redox peak from the PAH single-layer-coated ITO electrode. These results imply that the reversible charge trapping and release by PAH/ferritin multilayers originates in the ferritin NPs.

In contrast to the typical measurements of the electrochemical redox reaction of ferritin in aqueous solution recorded using CV, Xu *et* al. reported that a dry ferritin NP layer was 5–15 times more conductive than an apoferritin NP layer (i.e., ferritin without a ferrihydrite phosphate core).[22] Additionally, we cannot rule out the possibility that the protein shell, which contains amino acid residues, may have charge trapping properties, because various hydrophilic[40] and hydrophobic polymers[41] without transition-metal ions, such as Fe ions, have been used previously to prepare charge-trapping gate dielectrics for OFET memory devices despite their relatively low memory windows (<10 V). Building on these previous studies, we investigated the charge trap depth and stability of ferritin-based multilayers (**Figure 2**). This investigation is important in that the performance (particularly, the memory window and memory stability) of transistor memory devices depends strongly on achieving stable charge trapping in the gate dielectrics. Kelvin force microscopy (KFM) was used to examine the changes in real-space imaging of the charge trapping and release states of $(PAH/ferritin\ NP)_5$ and $(PAH/apoferritin\ NP)_5$ films as a function of time in air. The charges stored within each ferritin or apoferritin NP were detected from the change in the measured surface potential as the KFM tip, which was coated with Pt, scanned the surface of the ferritin or apoferritin NP multilayers while exposed to air. First, multilayer films with an area of $8 \times 8\ \mu m^2$ were scanned under a +10 V bias to search for a charge trap. The charge release operation was then performed by scanning an area of $5 \times 5\ \mu m^2$ under a –10 V bias, followed by scanning of an area of $2 \times 2\ \mu m^2$ at a +10 V bias. In Figure 2a, the yellow region identifies a charge trapping state in a ferritin NP multilayer, and the dark region corresponds to a charge release state. Note that these charge trap/release operations were reproducibly observed in a larger area ($23 \times 23\ \mu m^2$) than the $8 \times 8\ \mu m^2$ scanning area (SI, Figure S2). The potential difference between the charge trapping and release states was measured to be approximately 207 ± 3 mV However, the potential difference measured within the apoferritin NP multilayers was approximately 113 ± 5 mV, despite the use of identical measurement conditions. The potential differences within the ferritin or apoferritin multilayers were measured as a function of time to calculate the degree of charge trap decay (%). The charge storage state decayed more rapidly in the apoferritin multilayers than in the ferritin NP multilayers (Figure 2b). These

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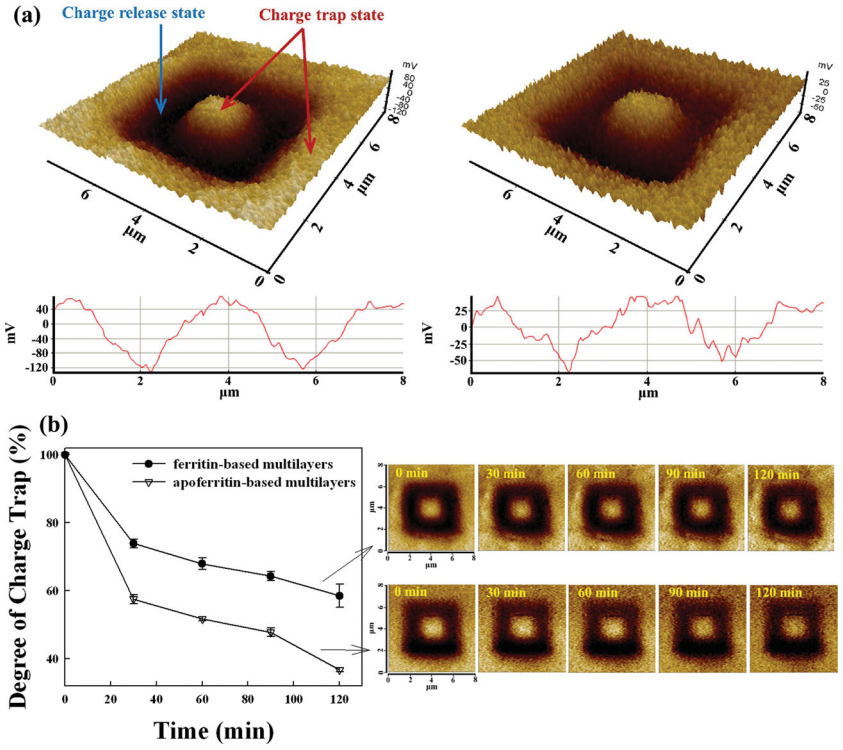

Figure 2. a) KFM images and voltage contrast data for the $(PAH/ferritin\ NP)_5$ and $(PAH/apoferritin\ NP)_5$ multilayers coated onto a Pt-coated Si wafer, measured from the charge trap/release operations. The voltage contrasts between the charge trapping and release states of the $(PAH/ferritin\ NP)_5$ and $(PAH/apoferritin\ NP)_5$ multilayers were measured to be approximately 207 and 113 mV, respectively. b) The degree of charge trap decay and KFM images of the PAH/ferritin NP and PAH/apoferritin NP multilayers as a function of time.

results indicate that the ferritin NPs with a ferrihydrite phosphate core formed deeper and more stable charge trapping states than apoferritin NPs with shallow charge trap sites. Furthermore, if the ferritin NP multilayers were sandwiched between SiO_2 and pentacene/source–drain electrodes that could block the formation of a contaminant layer (e.g., a surface water layer, a surface hydroxyl layer, or some other layer)[42] rather than being exposed to air, the charge trapping stability in the ferritin multilayers increased significantly (data supporting this assertion are presented below). However, we did not observe any significant change in the topographic images with increasing time (SI, Figure S3). It should also be noted that the charge trap/release states were not observed in a pure PAH layer.

These results were used to inform the fabrication of OFET memory devices based on ferritin NP multilayers. The observed output and transfer characteristics of the resultant ferritin-based devices indicated typical p-channel OFET behavior, which indicates that the insertion of thin multilayers between the SiO_2 gate dielectric and the pentacene layer did not significantly affect the performance of the OFET device (SI, Figure S4).[43,44] OFET devices based on ten bilayers exhibited a saturation field-effect mobility (μ_{FET}) of 0.013 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage (V_{th}) of 5.56 V, and an ON/OFF current ratio (I_{ON}/I_{OFF}) of 4×10^4, all of which are comparable to the values reported previously for pentacene transistors. A significant shift in V_{th} was observed after an appropriate gate voltage (V_G) was applied for a relatively short time (1 s), as shown in **Figure 3**a. That is, when the device was subjected to a programmed V_G of +100 V, the hole carriers injected from ferritin to the pentacene layer accumulated at the dielectric/organic interface to produce high conductivity and a positive V_{th} shift. With regard to the redox active sites of ferritins, the hole carriers were ejected from the ferrihydrite phosphate core in an initially oxidized form (i.e., Fe^{III}) into the pentacene layer. The application of a negative gate bias for erasure resulted in the transfer of the hole carriers at the pentacene/gate dielectric interface to the ferritin centers. The trapped hole charges in the ferritins built up an internal electric field that partially offset the external applied electric field and resulted in low conductivity and a negative V_{th} shift. In this case, the hole carriers injected from pentacene to the ferritin NPs produced a ferrihydrite phosphate core in a reduced form (i.e., Fe^{II}). However, these charge trap/release phenomena may partly originate from amino acid residues without Fe ions as well as the ferrihydrite phosphate core, as shown in KFM images of apoferritin NP-based multilayer films (these phenomena can be confirmed from the nonvolatile memory behavior of OFET memory devices based on PAH/apoferritin gate dielectrics and will be shown in the latter part of this paper). The number of trap charges can be calculated using the equation $\Delta n = C_i \cdot \Delta V_{th}/e$, where C_i and e are the specific capacitance of the gate dielectric (16.2 nF cm^{-2}) and the element charge, respectively.[45] Therefore, the total number of trapped charges in devices with ten bilayers was calculated to be approximately 2.5×10^{12} cm^{-2}; hence, one to two charge carriers were trapped in each ferritin NP.

Electrical bistability after application of a program (P)/erase (E) bias of $V_G = \pm 100$ V for 1 s (V_G = +100 and –100 V are defined as the "program" and "erase" voltages) was observed in all memory devices based on the $(PAH/ferritin\ NP)_{n=2-40}$ multilayered gate dielectrics. Shifts in the threshold voltage or memory window (defined as the difference in V_{th} after the application of P/E bias pulses for a given time period, that is, $\Delta V_{th} = V_{th,ERASE} - V_{th,PROGRAM}$) increased significantly as the gate voltage pulses were increased up to ±100 V; however, no significant changes in ΔV_{th} were observed above $V_G = \pm 100$ V (SI, Figure S5). Interestingly, ΔV_{th} increased as the bilayer number increased to 10, although further increases in the bilayer number slightly reduced ΔV_{th} (Figure 3b). The initial increase in ΔV_{th} mainly resulted from an increase in the surface coverage (charge trap sites) of ferritin molecules adsorbed onto the substrate during LbL assembly. Once the trap density had saturated, further increases in the dielectric multilayer thickness (i.e., increases

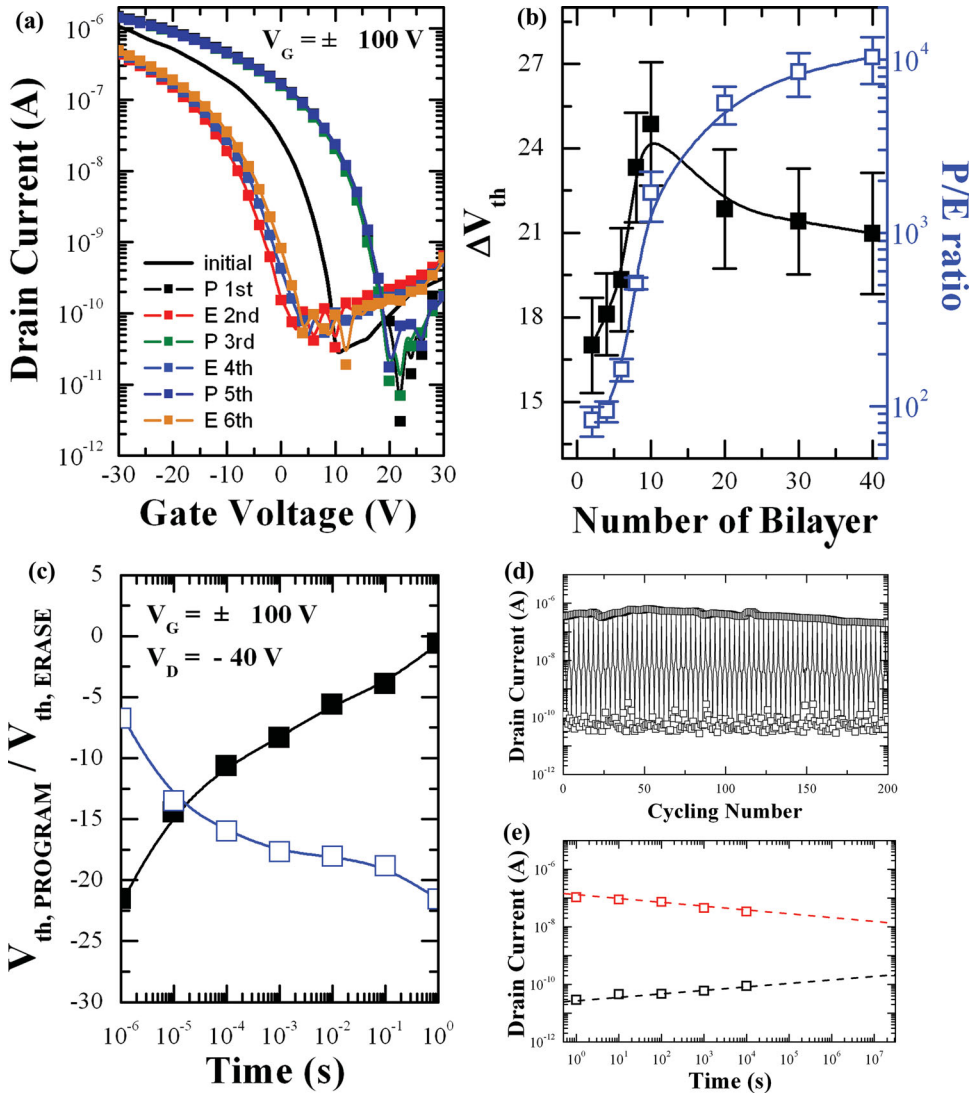

Figure 3. a) Shifts in the transfer curves at $V_D = -40$ V for OFET memory devices prepared using $(PAH/ferritin\ NP)_{10}$ gate dielectrics. b) Change in ΔV_{th} and P/E ratio for the memory devices as a function of the bilayer number (n) of $(PAH/ferritin\ NP)_n$ gate dielectrics, varied from 2 to 40. c) P/E speeds of the memory devices. d) Cycling and e) retention time tests for devices with $(PAH/ferritin\ NP)_{40}$ multilayers.

in the bilayer number) caused a decrease in the capacitance, and the memory window decreased because of a reduction in the number of trapped charges. However, the P/E drain current ratio (P/E ratio) of the devices increased from 8.3×10^1 to 1.0×10^4 without reaching a maximum level as the bilayer number increased because devices with thicker dielectrics produced lower OFF current levels (Figure 3b). The individual programming and erasing current level curves as a function of bilayer number are shown in the Supporting Information, Figure S6.

The P/E speeds of the devices were investigated, as shown in Figure 3c, and ±100 V programming and erasing bias pulses were applied to the gate electrode at pulse widths that varied from 1 to 10^{-6} s. In this case, a meaningful switching speed of the device was obtained for times above 10 μs. A 40-bilayer device with a relatively high P/E current ratio (1.0×10^4) yielded values of –0.61 and –21.6 V for $V_{th,PROGRAM}$ and $V_{th,ERASE}$, respectively, for 1 s. Although the shift in V_{th} decreased gradually as the P/E switching speed was decreased, a reasonable shift in V_{th} was obtained by applying a bias pulse longer than 10 μs. To further investigate the stability of the devices prepared using the ferritin gate dielectrics, retention time and cycling tests were performed. In these cases, the P/E states were maintained during repeated cycling tests, which included approximately 300 cycles with a switching speed of 1 s and a test period of 10^4 s in air (Figure 3d,e). Although the PAH/apoferritin NP multilayered devices also displayed transistor memory properties (SI, Figure S7), their performance was unstable, presumably because of the shallow charge trap states of the apoferritin NPs. Our approach was also extended to the preparation of memory devices with enzyme gate dielectrics (i.e., $(PAH/catalase)_n$ multilayers based on catalase with heme Fe^{III}/Fe^{II} redox couples; SI, Figure S8). Various biomaterial-based redox couples can thus be employed as charge trapping materials in transistor memory devices.

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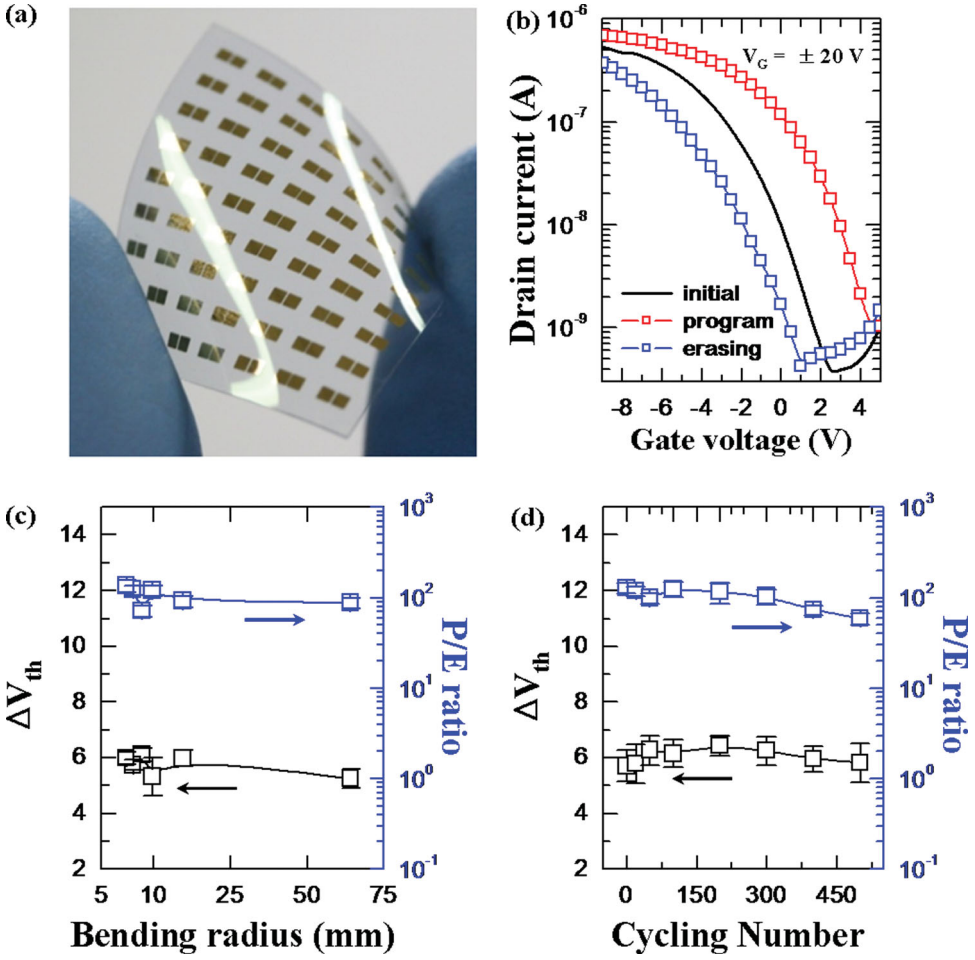

Figure 4. a) Photographic image of a flexible OFET memory device with 50-nm-thick Al_2O_3 and $(PAH/ferritin\ NP)_{10}$ gate dielectrics. b) Transfer curves for the flexible OFET memory devices (program voltage = +20 V and erasing voltage = −20 V, i.e., $V_G = \pm 20$ V). Mechanical stability tests for the flexible memory devices as a function of c) the bending radius and d) the bending cycling number. The bending cycling tests for flexible devices were performed by repeatedly bending the devices.

The devices described herein were manufactured at low temperatures (below 100 °C) and could be fabricated on a variety of substrates. Therefore, our approach can be effectively applied to the preparation of flexible OFET memory using plastic substrates. In an effort to realize flexible devices, a poly(ethylene naphthalate) sample was coated with an ITO gate electrode and a 50-nm-thick Al_2O_3 gate dielectric layer. The subsequent procedures for preparing an OFET memory device were identical to those used to prepare the silicon substrate-based devices. **Figure 4**a shows an optical microscopy image of a ferritin-based OFET memory array on a plastic substrate. The specific capacitance of the Al_2O_3 with $(PAH/ferritin)_{10}$ multilayers was 90.4 nF cm^{-2}. The high value of V_G required for programming and erasing (±100 V) was significantly reduced by using an Al_2O_3 gate dielectric layer (Figure 4b). It has been reported that OFET memory devices with low operating voltages could be prepared by using a high-k dielectric layer, such as HfO_2 or Al_2O_3.[46–49]

Electrical bistability of the devices was observed by sweeping the low gate voltage below 10 V after applying P/E gate voltages of ±20 V for 1 s, which suggests that the bistability resulted directly from the high capacitance of the Al_2O_3 gate dielectrics. In this case, ΔV_{th} and the P/E current ratio were found to be 7.14 V and 1.3×10^2, respectively. A memory window of 7.14 V was found and was comparable to that obtained in Si-based devices upon application of a V_G of ±50 V. Additionally, the programmed and erased states of the flexible film devices were observed to be stable in ambient air over a long duration (SI, Figure S9).

Mechanical flexibility and robustness are important characteristics for OFET memory device applications in flexible electronics. A symmetric bending test was performed on the OFET memory array. Figure 4c shows the changes in the memory window and P/E ratio during the bending tests. The memory devices on plastic substrates displayed excellent electrical stability, without significant change, as the bending radius was changed from 65 to 7 mm. A fatigue test conducted on the OFET memory devices showed that the ΔV_{th} and P/E ratio were invariant with bending along the longitudinal direction, even after 500 cycles (bending radius = 8.6 mm; Figure 4d). These results indicate that our approach, which uses protein interlayers, can be effectively applied to flexible OFET memory devices as well as Si-based devices.

3. Conclusion

We have designed a novel type of OFET memory device based on ferritin NP multilayers that displays nonvolatile memory properties as a result of reversible shifts in V_{th} arising from charge trapping and detrapping in the ferritin gate dielectric layers; furthermore, the memory switching properties of these devices originate from the incorporated ferritin NPs. These devices exhibited a large memory window (20 V), a high P/E current ratio (10^4), and good electrical reliability. These devices were effectively extended to flexible transistor memory devices to enable reliable electrical and mechanical stability. The use of plastic substrates in combination with high-k Al_2O_3 gate dielectrics enabled the low-voltage operation of flexible OFET memory devices. Bio-inspired memory devices that employ isolated and robust protein NP layers may provide a basis for the exploitation of novel types of charge storage gate dielectrics and the development of advanced flexible electronics.

4. Experimental Section

Materials: The ferritin (from bovine liver, Aldrich), PAH (M_w = 70 000, Aldrich), and PAA (M_w = 70 000, Aldrich) solutions used in all of the experiments had a concentration of 1 mg mL^{-1}.

Thermogravimetric Analysis of the PAH/Ferritin NP Nanocomposites: To confirm the thermal decomposition of PAH/ferritin NP multilayers, the electrostatically aggregated PAH/ferritin powder was first prepared such that a PAH/ferritin NP mass ratio of 1.0:2.7 was incorporated in an aqueous solution (the mass ratio of the powder was determined from the amount of PAH (i.e., Δm of approximately 392 ng cm^{-2}) and ferritin NPs (i.e., Δm of approximately 1085 ng cm^{-2}) adsorbed in the LbL multilayers; see the QCM results). These aggregated powders were sufficiently dried for 6 h under vacuum. After drying, the residual water of the aggregated powder was investigated by increasing the temperature to 150 °C at a heating rate of 5 °C min^{-1}. In this case, no change in mass was observed in the range from room temperature to 150 °C (SI, Figure S10). These results imply that the PAH/ferritin NP multilayers do not contain residual water after the vacuum drying process.

Preparation of OFET Memory Devices: Ferritin NP-based OFET memory devices (i.e., 200-nm-thick SiO_2/(PAH/ferritin)$_n$/pentacene/Au source/drain electrodes) were fabricated using a highly doped n-type Si wafer with a thermally grown 200-nm-thick SiO_2 layer as the substrate. N-type Si wafers were employed as the gate electrode, and an oxide layer was employed as the gate dielectric. Prior to treatment of the silicon oxide surface, the wafer was cleaned in piranha solution for 30 min at 100 °C and then washed with distilled water. PAH/ferritin NP multilayers were deposited onto the substrates (i.e., SiO_2-coated wafers) at pH 9 using an electrostatic LbL assembly process. The substrates were dipped for 10 min in the cationic PAH solution, washed twice by dipping in water for 1 min, and then air-dried under a gentle stream of nitrogen. Anionic ferritin NPs were subsequently deposited onto the PAH-coated substrates by using the same adsorption, washing, and drying procedures described above. This process was repeated until the desired number of layers was deposited. The resultant multilayer films were dried under vacuum conditions.

Pentacene (Aldrich Chemical Co., no purification) films with a thickness of 50 nm were deposited onto the PAH/ferritin NP multilayers at a rate of 0.2 Å s^{-1} using an organic molecular beam deposition system. The devices were completed by evaporating gold through a shadow mask to define the source and drain contacts on the pentacene film with channel length and width values of 100 and 800 μm, respectively.

A plasma-enhanced atomic layer deposition-assisted 50-nm-thick Al_2O_3 gate dielectric layer was prepared on ITO-coated poly(ethylene naphthalate) to produce a flexible OFET memory device for low-voltage operation. Trimethylaluminum and O_2 were used as the precursors for Al and O, respectively. The film was grown on the substrate at a temperature of 100 °C in a reactor under a radio-frequency power of 100 W, using Ar as a carrier gas.

QCM Measurement: A QCM device (QCM200, SRS) was used to characterize the mass of material deposited after each adsorption step. Although Kasemo et al. reported that the application of the Sauerbrey equation, between the adsorbed mass and frequency change, is difficult for a viscoelastic, thicker, or hydrogel layer containing water molecules in its solid/liquid interface,[50] the QCM measurements in our study were obtained after sufficient drying of the adsorbed layers using nitrogen gas.[30] Therefore, the PAH and ferritin layers adsorbed on the crystal surface may be regarded as rigid, evenly distributed, and sufficiently thin films satisfying the Sauerbrey equation:

$$\Delta F\,(\mathrm{Hz}) = -\frac{2F_0^2}{A\sqrt{\rho_q \mu_q}} \cdot \Delta m$$

Here, F_0 (approximately 5 MHz) is the fundamental resonant frequency of the crystal, A is the electrode area, and ρ_q (approximately 2.65 g cm^{-2}) and μ_q (approximately 2.95×10^{11} g cm^{-2} s^{-2}) are the shear modulus and density of quartz, respectively. This equation can be simplified as follows:

$$\Delta F\,(\mathrm{Hz}) = -56.6 \times \Delta m_A$$

where Δm_A is the mass change per quartz crystal unit area in μg cm^{-2}. As a result, the adsorbed mass of PAH and ferritin, Δm, can be calculated from the change in QCM frequency, ΔF. The frequency values were measured more than five times per layer.

Film Thickness Measurement: The total film thickness of the (PAH/ferritin NP)$_n$ multilayers deposited onto the Si wafer was measured using cross-sectional images obtained by field-emission scanning electron microscopy (S-4300, Hitachi). The thickness was averaged from values measured at ten different regions.

HRTEM Measurement: The size and number density of ferritin NPs deposited onto a PAH-coated carbon grid were determined using HRTEM (Tecnai G2 F20, Philips). The PAH-coated carbon grid was prepared as follows: the carbon grid was first deposited in the PAH solution (1 mg mL^{-1}) for 10 min and then washed in water. After washing, the PAH-coated grids were dried using a gentle nitrogen stream.

KFM Measurement: The real-space (for the charge trapping and release states) and topographic images of the (PAH/ferritin NP)$_5$ and (PAH/apoferritin NP)$_5$ films were obtained using Kelvin force microscopy (KFM; XE-100, Parksystem). The potential difference between the charge trapping and release states was measured in five different regions of one image.

Cyclic Voltammetry Measurement: The electrochemical properties of ferritin NP multilayer films adsorbed onto ITO electrodes were investigated using CV (Compactstat, IVIUM).

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I–V Characterization: The current–voltage (*I–V*) characteristics of the OFET memory devices were measured at room temperature under ambient conditions in a dark environment using a Keithley 4200 Semiconductor Parameter Analyzer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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