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Supporting Information

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Organic Field-Effect Transistor Memory Devices Using Discrete Ferritin Nanoparticle-Based Gate Dielectrics

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Supporting Information

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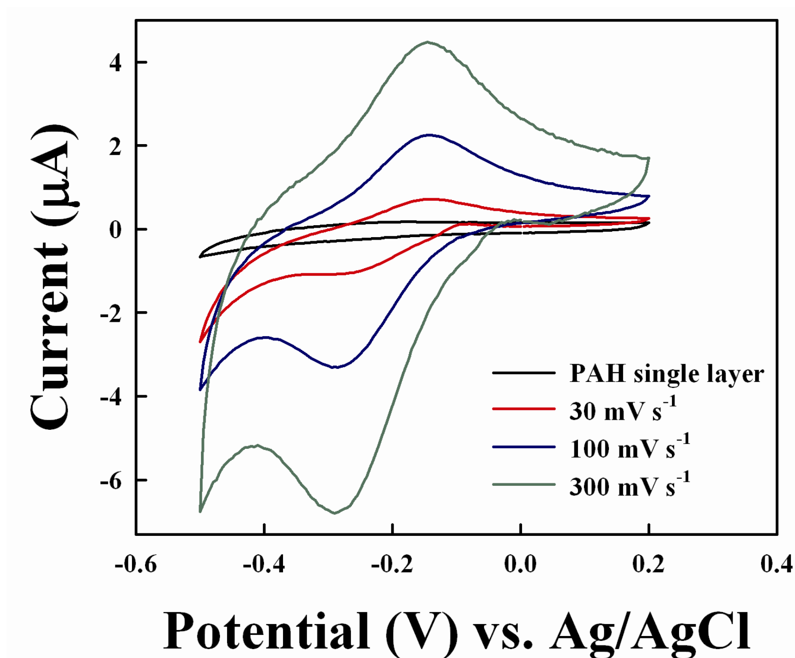

Figure S1. Cyclic voltammograms from PAH/ferritin multilayer-coated indium tin oxide electrodes with electrode area of 0.5 cm^2 in phosphate buffer solutions at pH 7 (potential sweep rates: 3, 100, and 300 $mV{\cdot}s^{-1}$). In the case of PAH single layer, the scan rate was 100 $mV{\cdot}s^{-1}$.

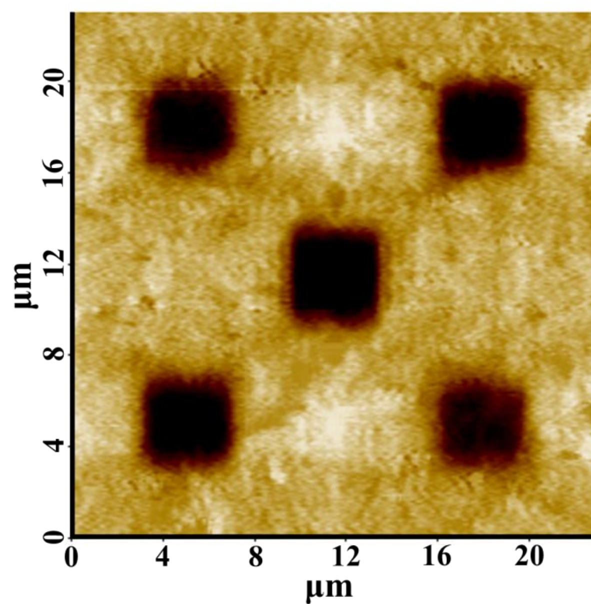

Figure S2. KFM image for the (PAH/ferritin NP)$_5$ multilayers coated onto a Pt-coated Si wafer, measured from the charge trap/release operations. First, 23 x 23 μm^2 area were scanned under + 10 V bias for a charge trap. The charge release operation was then performed by scanning five different regions of 3 x 3 μm^2 area under – 10 V bias. These results imply that charge trap/release operations are uniformly observed in the total film area.

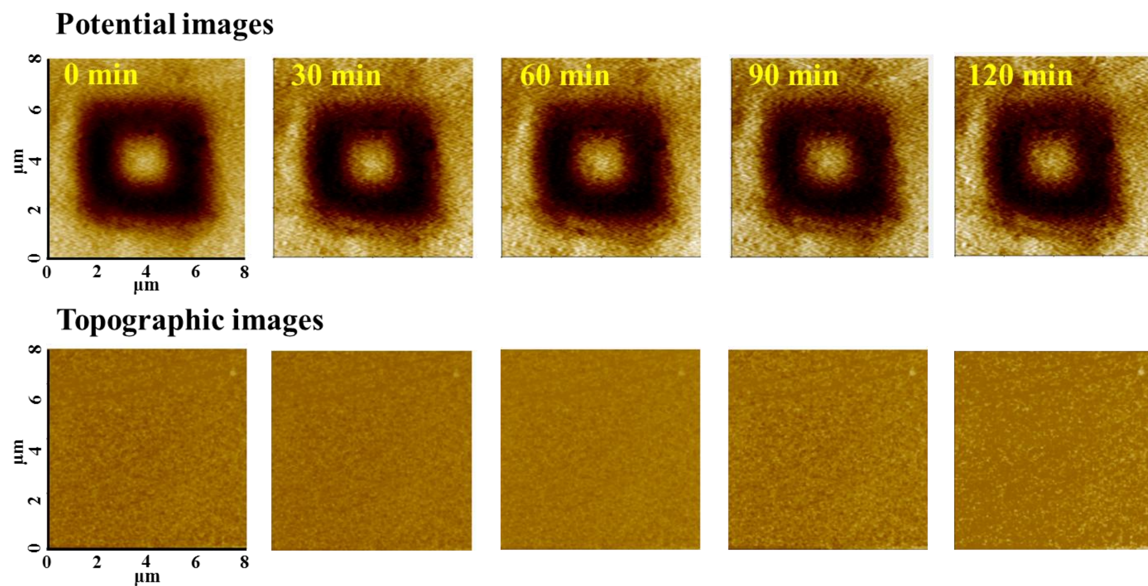

Figure S3. 2D-topographic images of (PAH/ferritin NP)$_5$ multilayer films as a function of time shown in Figure 2b. These results imply that topographic images of multilayers are not changed by charge trap (+10 V)/release (-10 V) operations under the given bias condition.

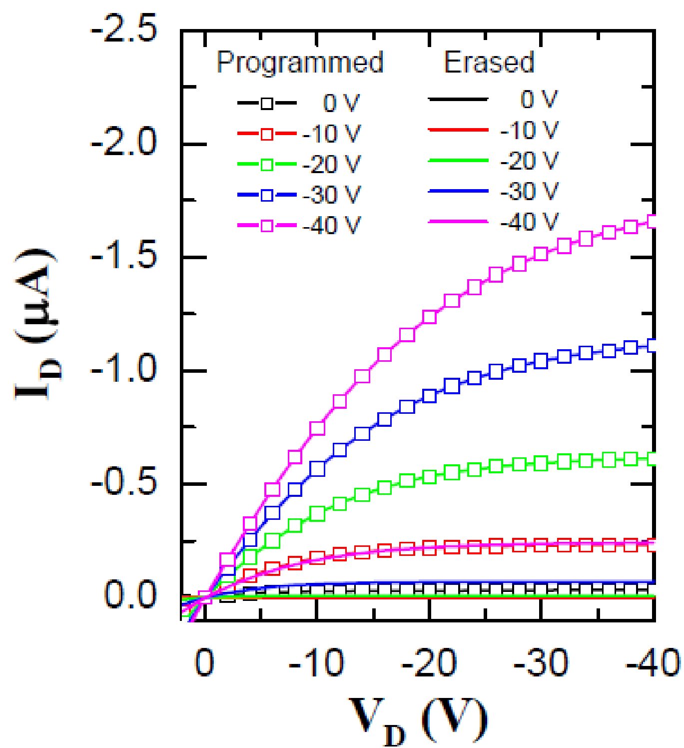

Figure S4. Output characteristics of OFET memory devices with (PAH/ferritin NP)$_{10}$ multilayered gate dielectrics. The curves were obtained after applying V_G = + 100 V for programming, and V_G = -100 V for erasing (1 s).

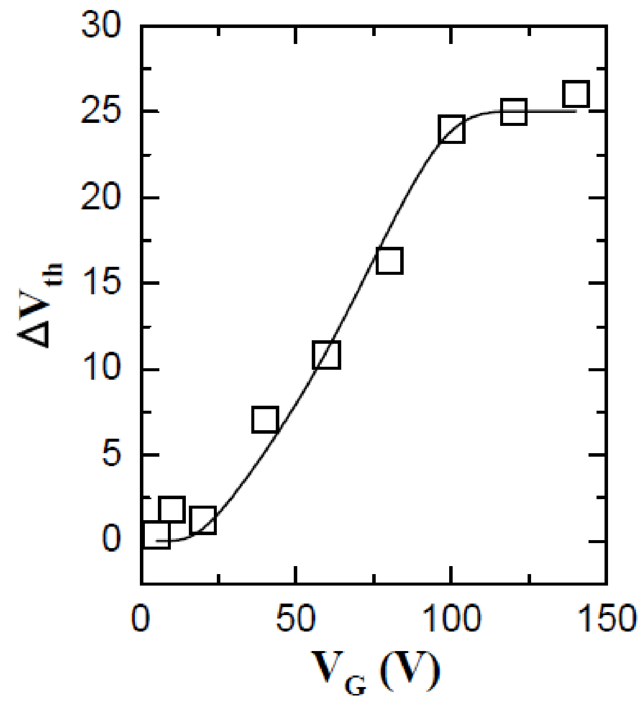

Figure S5. Memory window (ΔV_{th}) characteristics of ferritin NP multilayer-based OFET device as a function of programming and erasing voltages.

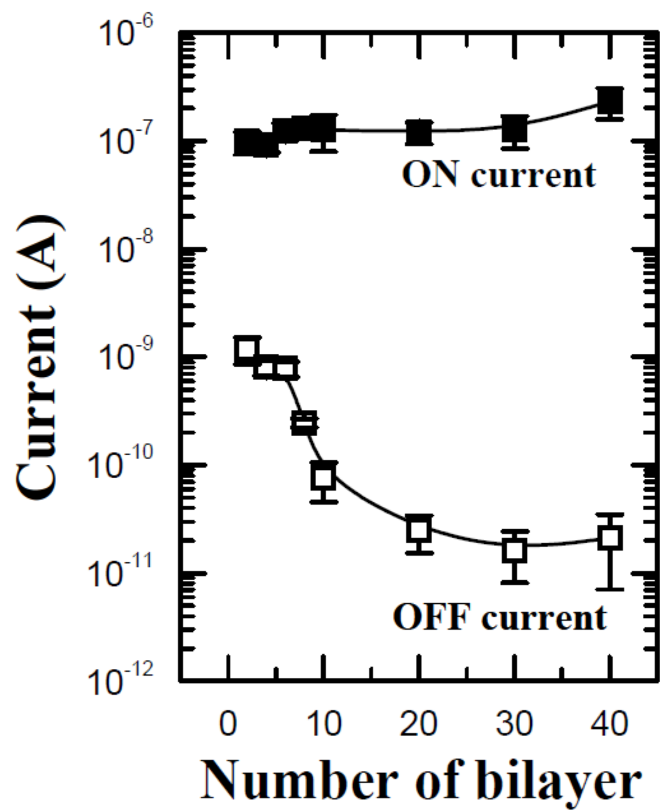

Figure S6. Change in programming and erasing current level for memory devices as a function of the bilayer number (n) of $(PAH/ferritin\ NP)_n$ gate dielectrics, varied from 2 to 40.

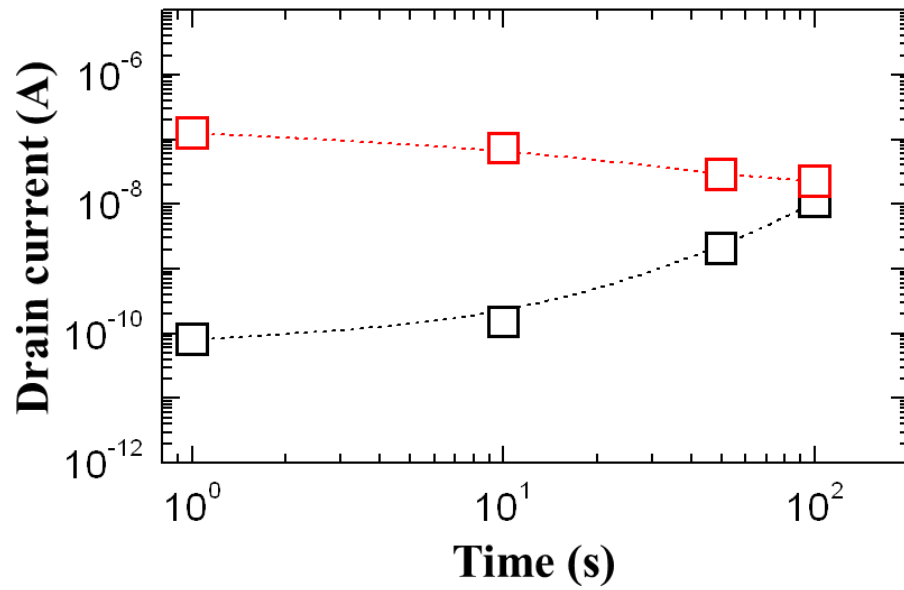

Figure S7. Retention time test for pentacene OFET memory devices with (PAH/apoferritin NP)$_{10}$ gate dielectrics. V_G = + 100 V for programming and V_G = -100 V for erasing were applied for 1 s.

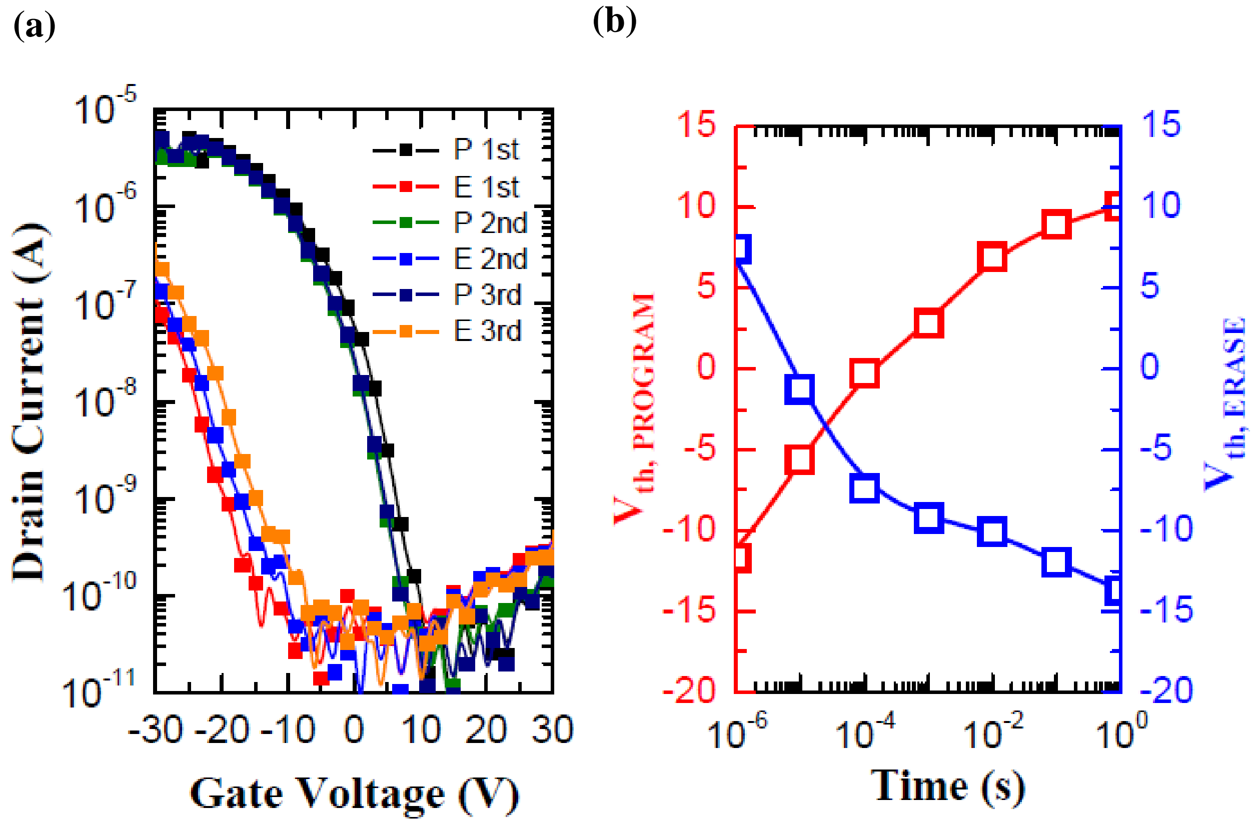

Figure S8. (a) Shifts in transfer curves at V_D = -40 V for pentacene OFET memory devices with (PAH/catalase)$_{30}$ gate dielectrics. V_G = + 100 V for programming and V_G = -100 V for erasing were applied for 1 s. (b) Program/erase speeds of pentacene OFET memory devices with (PAH/catalase)$_{30}$ gate dielectrics. Programming/erasing bias pulses of V_G = ± 100 V were applied to the gate at different pulse widths.

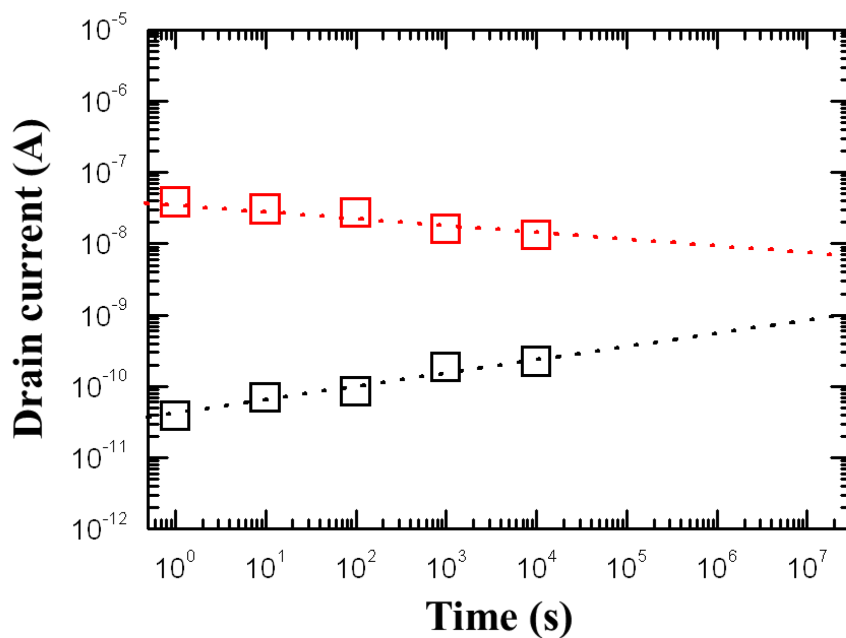

Figure S9. Retention time tests for the plastic film devices with (PAH/ferritin NP)$_{40}$ multilayers. The device structure is as follows: ITO-coated PEN/Al_2O_3 gate dielectric/(PAH/ferritin NP)$_{40}$ multilayers/Pentacene/source-drain electrode.

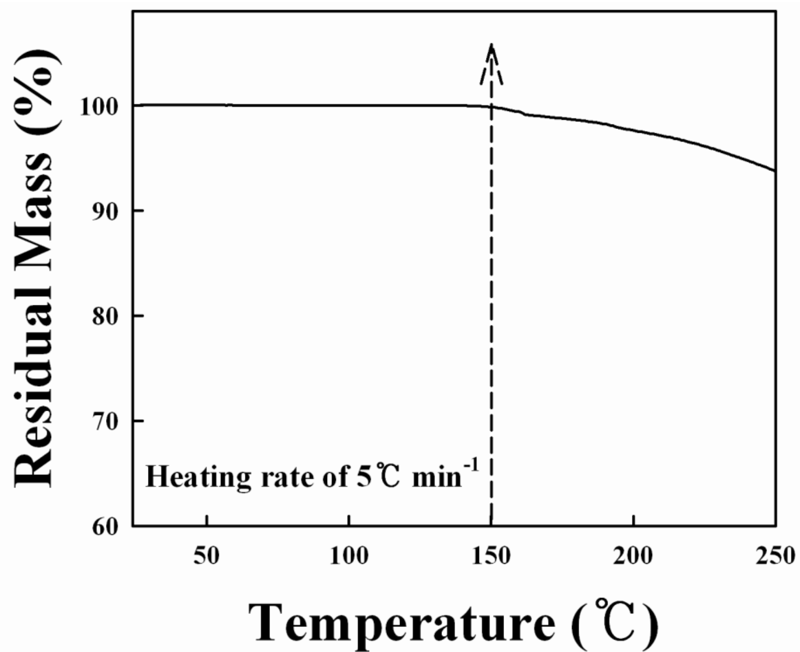

Figure S10. Thermogravimetric analysis (TGA) data of PAH/ferritin nanocomposites.